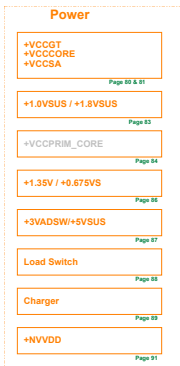


### BLOCK DIAGRAM

( UA : UMA )  
( UR : DGPU = Nvidia N16S\_GMR )  
( UQ : DGPU = Nvidia N16S\_GTR )



Use as GPO N/A  
GPIO setting to  
GPO low

PCH\_CPT  
GPIO

PCI_DEVICE_ID	Dev Ac	Signal Name	Power on Default State	IOA Dev Pin-Header	Power
0FF_00	0A00	BA0000	20_150	000 70 100	+30V
0FF_01	0A00	BA0000	LPC_A00		+30V
0FF_02	0A00	BA0000	LPC_A01		+30V
0FF_03	0A00	BA0000	LPC_A02		+30V
0FF_04	0A00	BA0000	LPC_A03		+30V
0FF_05	0A00	BA0000	LPC_FRAMES		+30V
0FF_06	0A00	BA0000	LPC_FRM002		+30V
0FF_07	000	0/A			+30V
0FF_08	BA0000	EN_CLEARDI			+30V
0FF_09	BA0000	EN_CLEARDI			+30V
0FF_10	BA0000	EN_CLEARDI			+30V
0FF_11	BA0000	EN_CLEARDI			+30V
0FF_12	BA0000	EN_CLEARDI			+30V
0FF_13	BA0000	EN_CLEARDI			+30V
0FF_14	BA0000	EN_CLEARDI			+30V
0FF_15	BA0000	EN_CLEARDI			+30V
0FF_16	BA0000	EN_CLEARDI			+30V
0FF_17	000	0/A			+30V
0FF_18	000	0/A			+30V
0FF_19	000	0/A			+30V
0FF_20	000	0/A			+30V
0FF_21	000	0/A			+30V
0FF_22	000	0/A			+30V
0FF_23	000	0/A			+30V
0FF_24	000	0/A			+30V
0FF_25	BA0000	EN_CLEARDI			+30V
0FF_26	000	0/A			+30V
0FF_27	000	0/A			+30V
0FF_28	000	0/A			+30V
0FF_29	000	0/A			+30V
0FF_30	000	0/A			+30V
0FF_31	BA0000	EN_CLEARDI			+30V
0FF_32	BA0000	EN_CLEARDI			+30V
0FF_33	BA0000	EN_CLEARDI			+30V
0FF_34	BA0000	EN_CLEARDI			+30V
0FF_35	BA0000	EN_CLEARDI			+30V
0FF_36	BA0000	EN_CLEARDI			+30V
0FF_37	BA0000	EN_CLEARDI			+30V
0FF_38	BA0000	EN_CLEARDI			+30V
0FF_39	BA0000	EN_CLEARDI			+30V
0FF_40	BA0000	EN_CLEARDI			+30V
0FF_41	BA0000	EN_CLEARDI			+30V
0FF_42	BA0000	EN_CLEARDI			+30V
0FF_43	BA0000	EN_CLEARDI			+30V
0FF_44	BA0000	EN_CLEARDI			+30V
0FF_45	BA0000	EN_CLEARDI			+30V
0FF_46	BA0000	EN_CLEARDI			+30V
0FF_47	BA0000	EN_CLEARDI			+30V
0FF_48	BA0000	EN_CLEARDI			+30V
0FF_49	BA0000	EN_CLEARDI			+30V
0FF_50	000	0/A			+30V
0FF_51	000	0/A			+30V
0FF_52	000	0/A			+30V
0FF_53	000	0/A			+30V
0FF_54	000	0/A			+30V
0FF_55	000	0/A			+30V
0FF_56	000	0/A			+30V
0FF_57	000	0/A			+30V
0FF_58	000	0/A			+30V
0FF_59	000	0/A			+30V
0FF_60	000	0/A			+30V
0FF_61	000	0/A			+30V
0FF_62	000	0/A			+30V
0FF_63	000	0/A			+30V
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0FF_67	000	0/A			+30V
0FF_68	000	0/A			+30V
0FF_69	000	0/A			+30V
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0FF_76	000	0/A			+30V
0FF_77	000	0/A			+30V
0FF_78	000	0/A			+30V
0FF_79	000	0/A			+30V
0FF_80	000	0/A			+30V
0FF_81	000	0/A			+30V
0FF_82	000	0/A			+30V
0FF_83	000	0/A			+30V
0FF_84	000	0/A			+30V

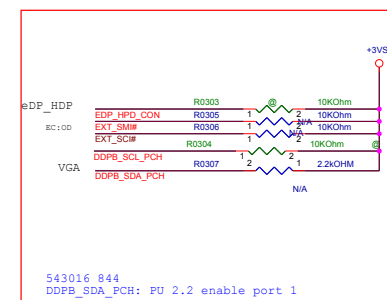
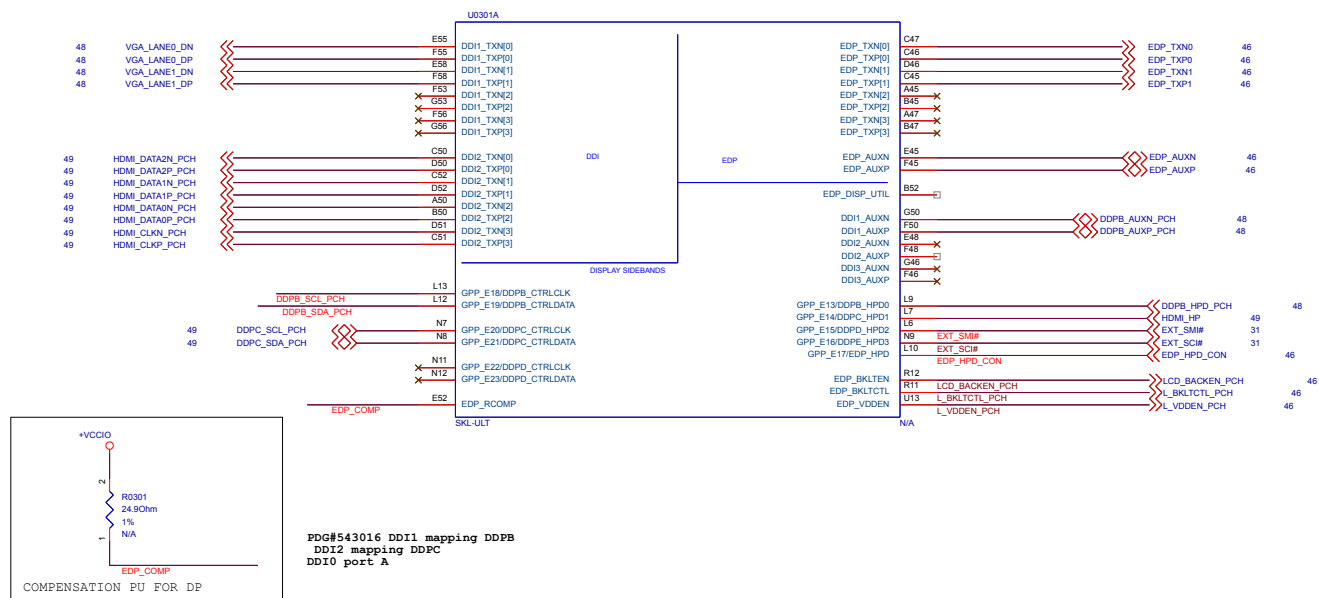
PGA_MODEL	QFN	Die As	Signal Name	Power on Default State	PGA Pin Polarity (I/O)	Power
QFP_001	QFN	N/A				
QFP_002	QFN	STRAP_BIASA, STRAPB_A			QFN Pin 10	+1.5V
QFP_003	QFN	STRAP_BIASB, STRAPB_B	N/A		QFN Pin 10	+1.5V
QFP_004	QFN	N/A			QFN Pin 10	+1.5V
QFP_005	QFN	N/A				
QFP_006	QFN	N/A				
QFP_007	QFN	N/A				
QFP_008	QFN	N/A				
QFP_009	QFN	N/A				
QFP_010	QFN	N/A				
QFP_011	QFN	N/A				
QFP_012	QFN	N/A				
QFP_013	NATIVE	STRAP_BIASA			QFN Pin 10	+1.5V
QFP_014	NATIVE	QFN_001			QFN Pin 10	+1.5V
QFP_015	QFN	STRAP_BIASB			QFN Pin 10	+1.5V
QFP_016	QFN	STRAP_BIASB			QFN Pin 10	+1.5V
QFP_017	NATIVE	STRAP_BIASB			QFN Pin 10	+1.5V
QFP_018	NATIVE	STRAP_BIASB			QFN Pin 10	+1.5V
QFP_019	NATIVE	STRAP_BIASB			QFN Pin 10	+1.5V
QFP_020	NATIVE	STRAP_BIASB			QFN Pin 10	+1.5V
QFP_021	NATIVE	STRAP_BIASB			QFN Pin 10	+1.5V
QFP_022	QFN	N/A				
QFP_023	QFN	N/A				
QFP_024	QFN	N/A				
QFP_025	QFN	N/A				
QFP_026	QFN	N/A				
QFP_027	QFN	N/A				
QFP_028	QFN	N/A				
QFP_029	QFN	N/A				
QFP_030	QFN	N/A				
QFP_031	QFN	N/A				
QFP_032	QFN	N/A				
QFP_033	QFN	N/A				
QFP_034	QFN	N/A				
QFP_035	QFN	N/A				
QFP_036	QFN	N/A				
QFP_037	QFN	N/A				
QFP_038	QFN	N/A				
QFP_039	QFN	N/A				
QFP_040	QFN	N/A				
QFP_041	QFN	N/A				
QFP_042	QFN	N/A				
QFP_043	QFN	N/A				
QFP_044	QFN	N/A				
QFP_045	QFN	N/A				
QFP_046	QFN	N/A				
QFP_047	QFN	N/A				
QFP_048	QFN	N/A				
QFP_049	QFN	N/A				
QFP_050	QFN	N/A				
QFP_051	QFN	N/A				
QFP_052	QFN	N/A				
QFP_053	QFN	N/A				
QFP_054	QFN	N/A				
QFP_055	QFN	N/A				
QFP_056	QFN	N/A				
QFP_057	QFN	N/A				
QFP_058	QFN	N/A				
QFP_059	QFN	N/A				
QFP_060	QFN	N/A				
QFP_061	QFN	N/A				
QFP_062	QFN	N/A				
QFP_063	QFN	N/A				
QFP_064	QFN	N/A				
QFP_065	QFN	N/A				
QFP_066	QFN	N/A				
QFP_067	QFN	N/A				
QFP_068	QFN	N/A				
QFP_069	QFN	N/A				
QFP_070	QFN	N/A				
QFP_071	QFN	N/A				
QFP_072	QFN	N/A				
QFP_073	QFN	N/A				
QFP_074	QFN	N/A				
QFP_075	QFN	N/A				
QFP_076	QFN	N/A				
QFP_077	QFN	N/A				
QFP_078	QFN	N/A				
QFP_079	QFN	N/A				
QFP_080	QFN	N/A				
QFP_081	QFN	N/A				
QFP_082	QFN	N/A				
QFP_083	QFN	N/A				
QFP_084	QFN	N/A				
QFP_085	QFN	N/A				

# Main Board

## Display Port

A	EDP
B	VGA
C	HDMI

Intel Version	ASUS P/N

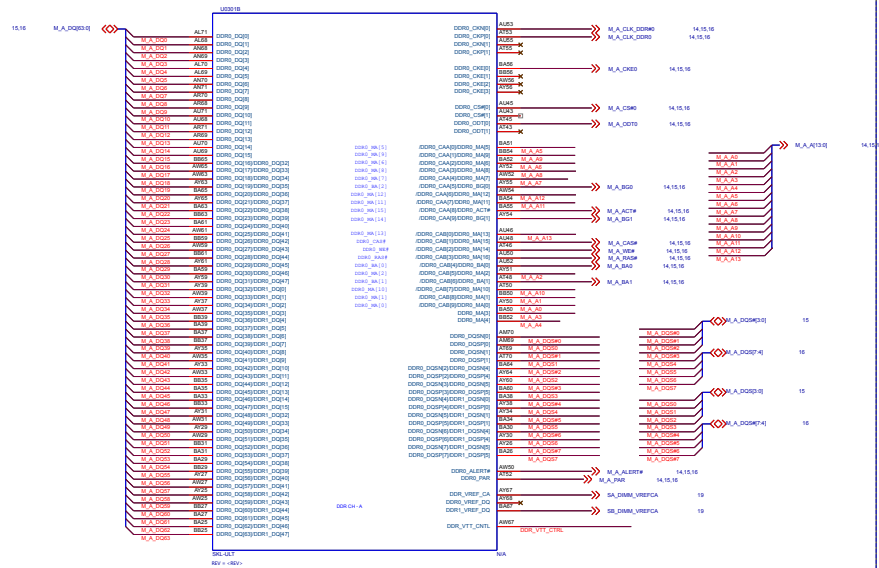


## BOM

Project Name		Rev
ASUS X442U		R1.0
Title : CPU_DISPLAY		
Size	Dept.: ASUSTek COMPUTER INC.	Engineer: SZ/EE
Custom	Date: Friday, October 13, 2017	Sheet 4 of 103

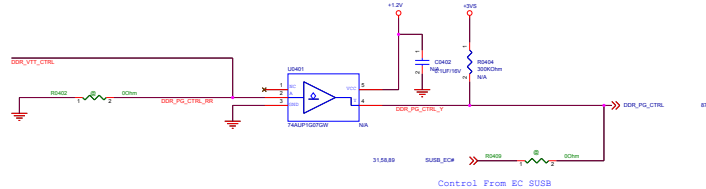
### Main Board

Memory Channel A

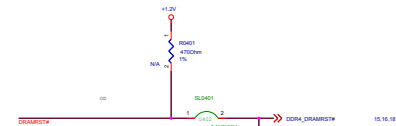
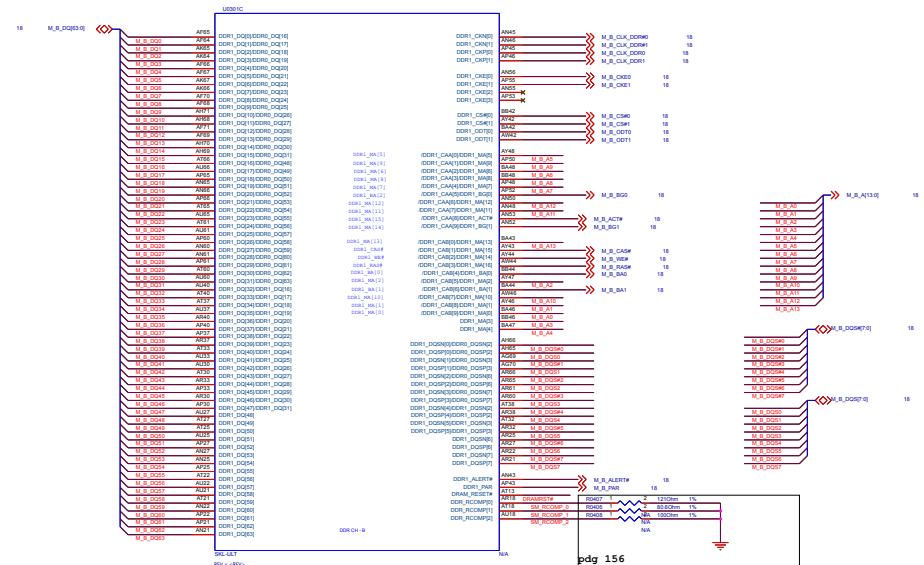


**DOR\_VTT\_CTRL:**  
System Memory Power Gate Control:  
Disables the platform memory VTT regulator  
in C8 and deeper and S3.  
Ref:544924\_544924\_Skylake\_EDS\_Vol\_1\_Rev0.9.pdf P.120

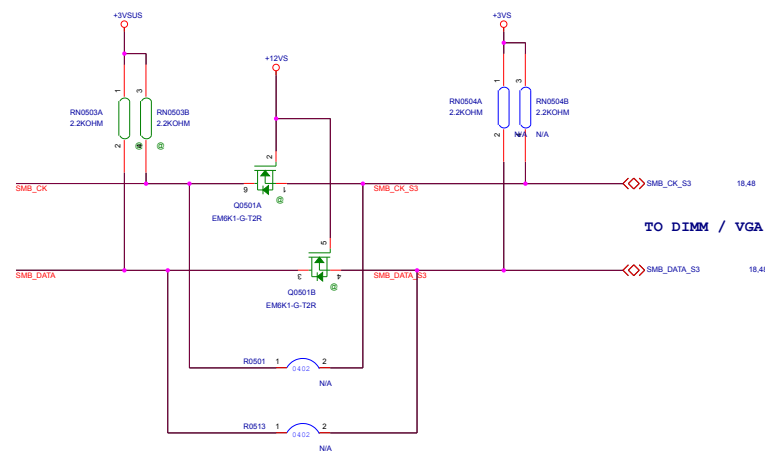
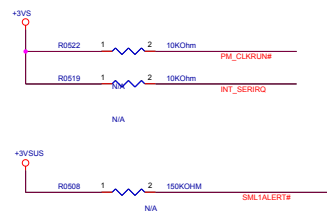
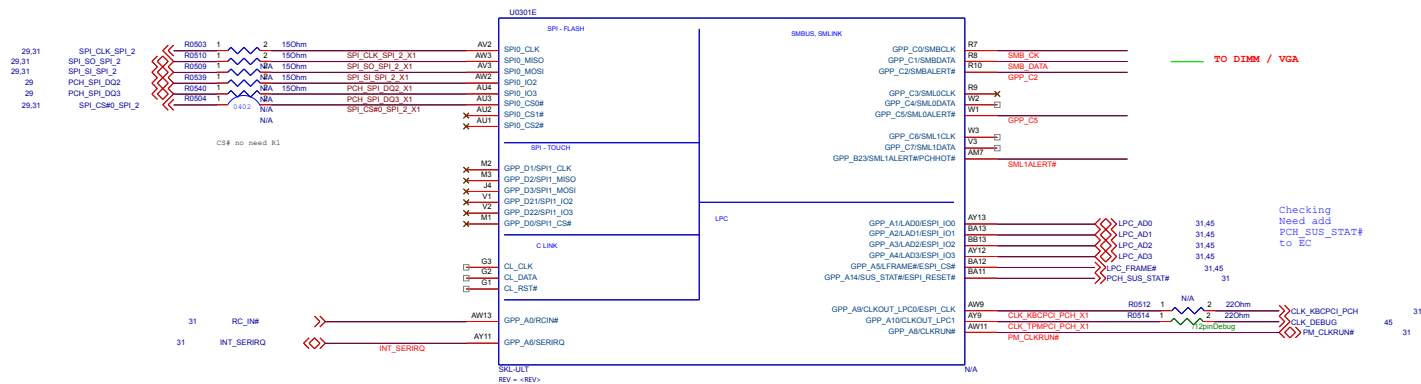
VTT Enable



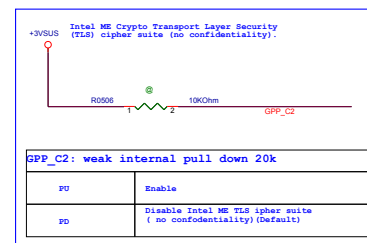
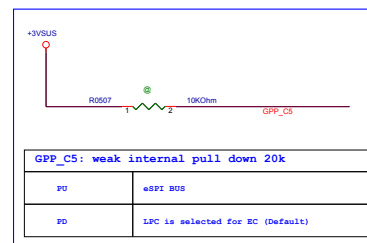
## Memory Channel B

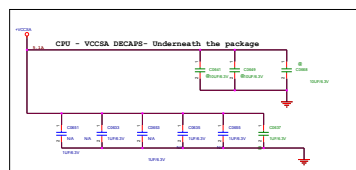
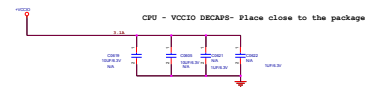
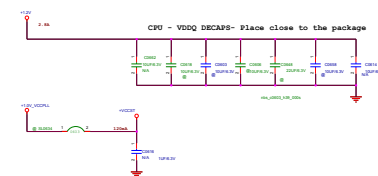
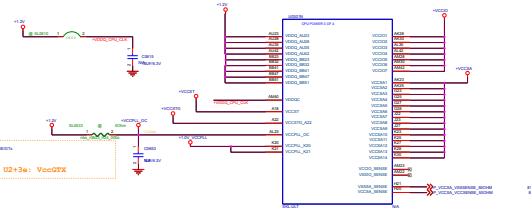
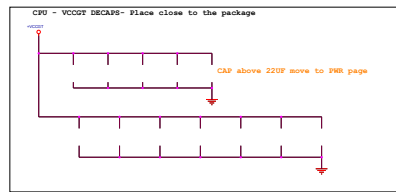
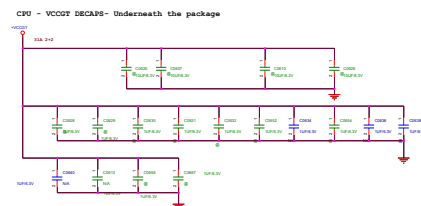
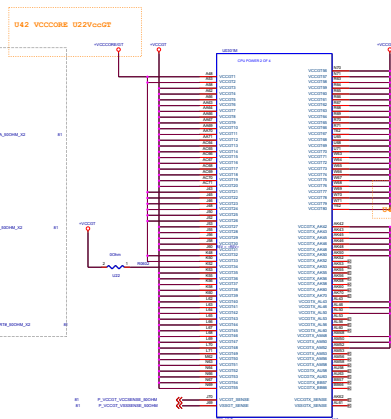
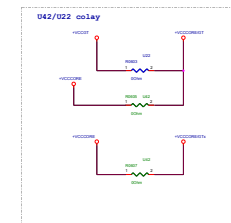
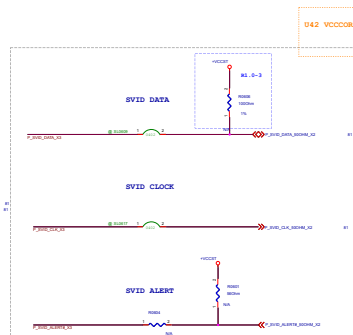
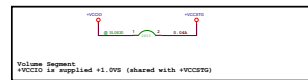
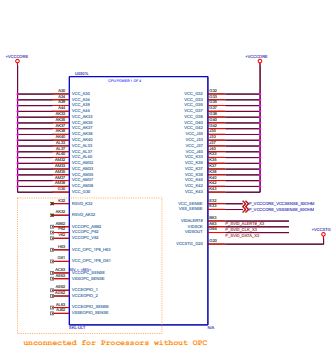


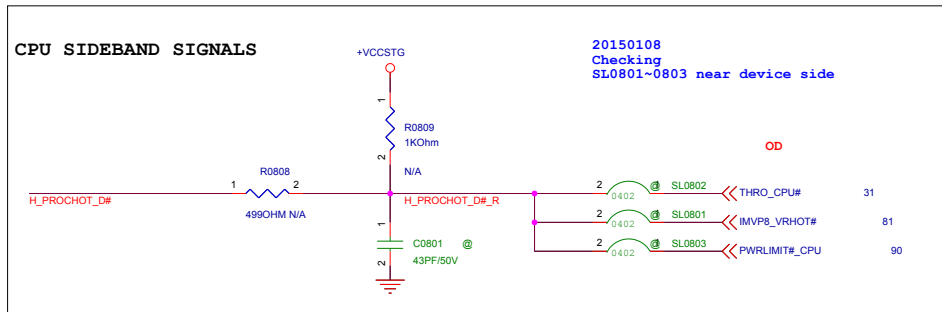
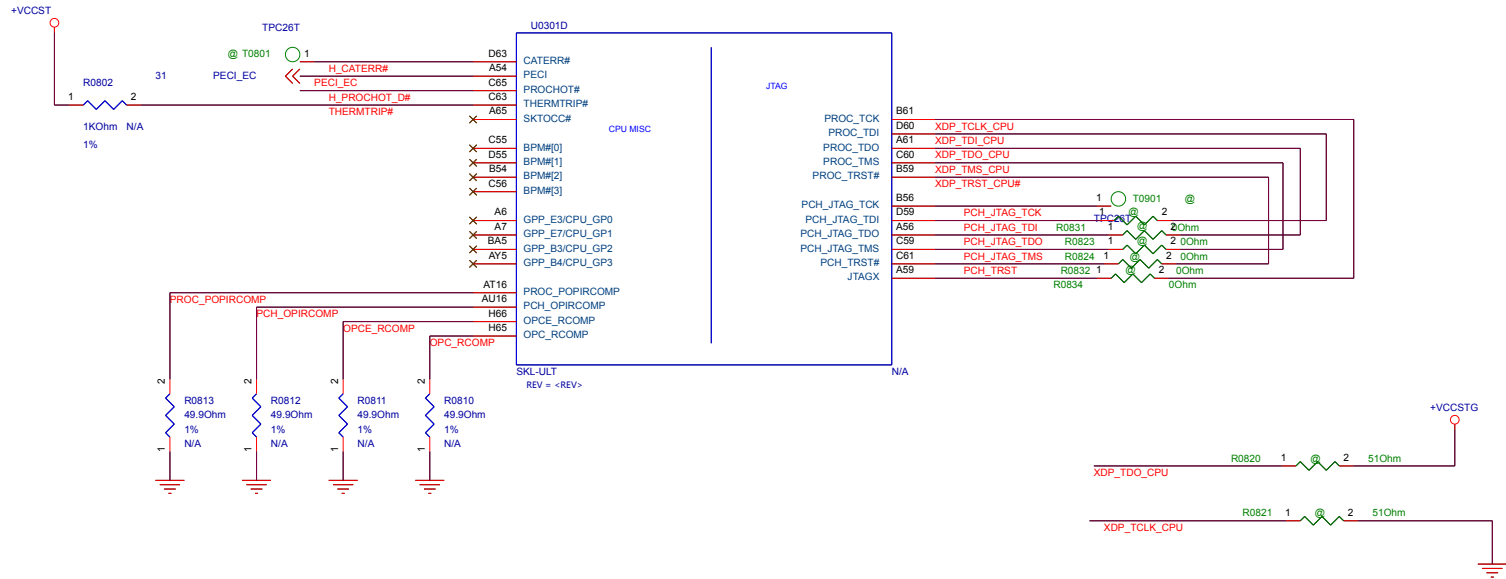
## Main Board



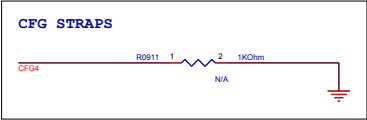
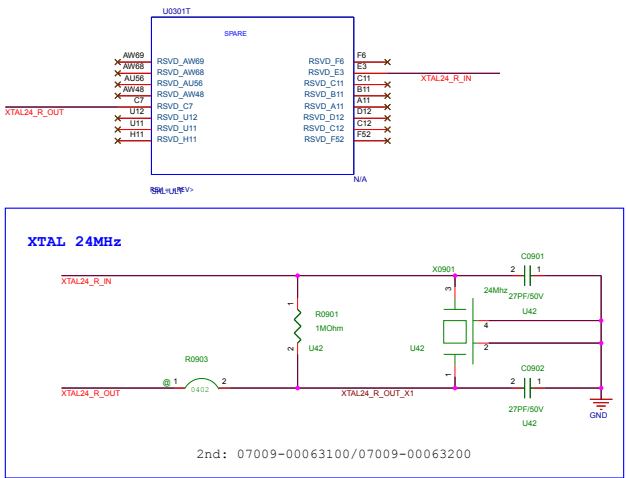
```
SML1ALERT# /PCHHOT#/GPP_B23
LOW during strap sampling:internal 20K PD;
When used as PCHHOT#, a 150k weak board
pull-up is recommended ;
```








## Main Board

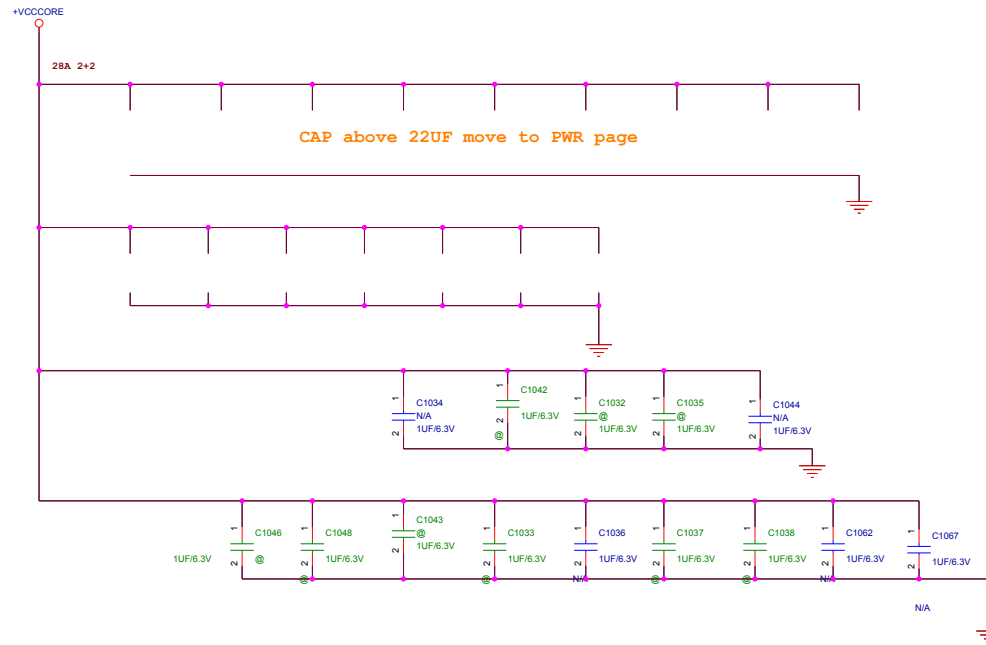


	1	0	NOTE
CFG4	DISABLE	ENABLE	eDP ENABLE

		Project Name		Rev	
		X442UV		R1.0	
Title : CPU_CFG,RSVD					
Size Custom		Dept.: ASUSTek COMPUTER INC.		Engineer: SZ/EE	
Date: Friday, October 13, 2017			Sheet 10 of 103		



CPU - VCC DECAPS- Underneath the package



CPU - VCC DECAPS- Place close to the package

CAP above 22uF move to PWR page

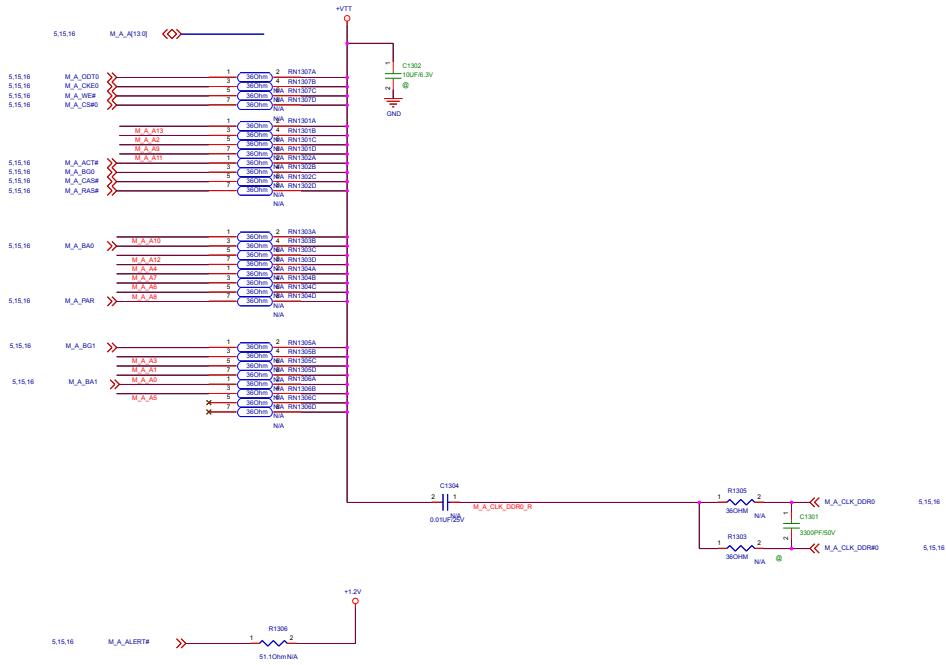
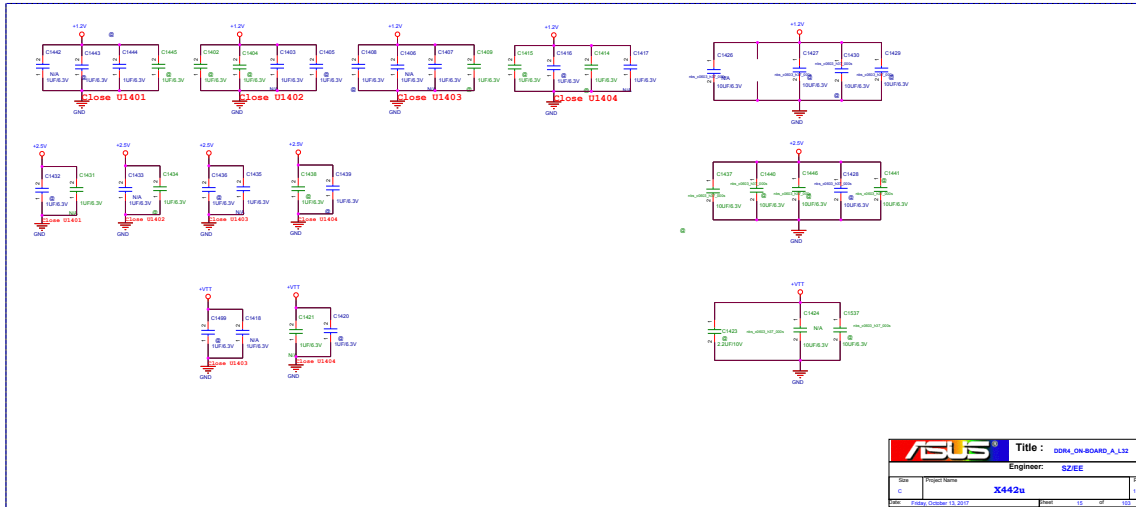
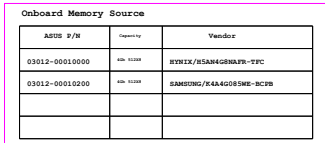


Table 4-2. System Memory Interface Guideline Terminology and Descriptions

SKL Processor and Memory Type	SKL H			
	DDR4/-RS SO-DIMM+ECC	DDR4/-RS SO-DIMM no ECC	DDR4/-RS Memory Down	LPDDR3 Memory Down
Signal Group Details				
Clock (CLK)	CKN[3:0], CKP[3:0]	CKN[3:0], CKP[3:0]	CKN[1:0], CKP[1:0]	CKP[1:0], CKN[1:0]
Control (CTRL)	CS#[3:0], ODT[3:0]	CS#[3:0], ODT[3:0]	CS#[1:0], ODT[1:0]	CS#[1:0], ODT[0]
Clock Enable (CKE)	CKE[3:0]	CKE[3:0]	CKE[1:0]	CKE[3:0]
Command (CMD)	MA[16:0], BG[1:0], BA[1:0], ACT#, PAR	MA[16:0], BG[1:0], BA[1:0], ACT#, PAR	MA[16:0], BG[1:0], BA[1:0], ACT#, PAR	CAA[9:0], CAB[9:0]
Strobe	DQSP[7:0], DQSN[7:0]	DQSP[7:0], DQSN[7:0]	DQSP[7:0], DQSN[7:0]	DQS[7:0], DQS#[7:0]
ECC strobe	DQSP[8], DQSN[8]	N/A	N/A	N/A
Data	DQ[63:0]	DQ[63:0]	DQ[63:0]	DQ[63:0]
ECC Data	DQ[71:64]	N/A	N/A	N/A
Alert	ALERT#	ALERT#	ALERT#	N/A
Reset	DRAM_RESET#	DRAM_RESET#	DRAM_RESET#	N/A
RCOMP	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]





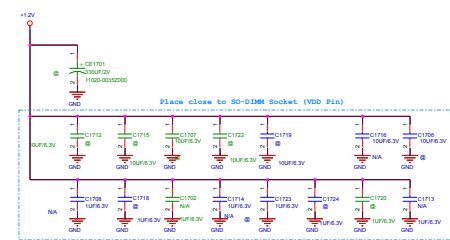
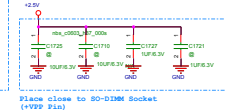
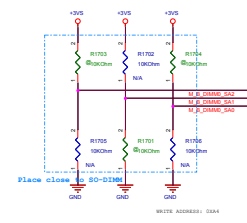
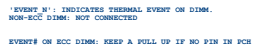


Figure 4-51. SKL U DDR4/-RS x8 Devices Memory Down V<sub>REF-CA</sub> Overview

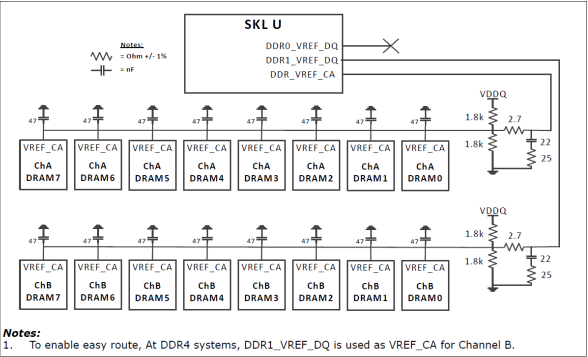
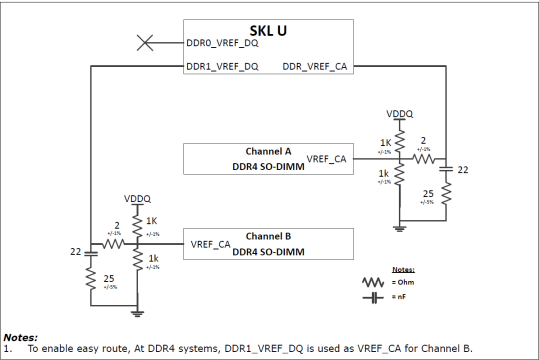
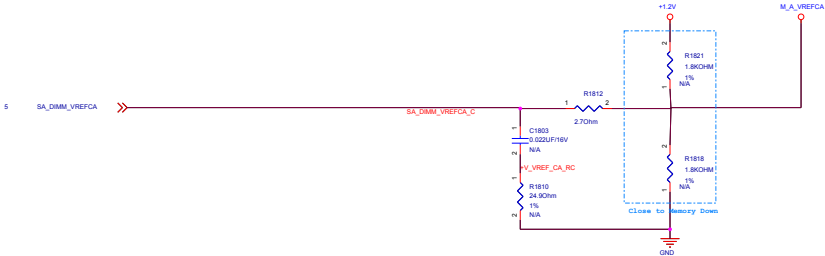
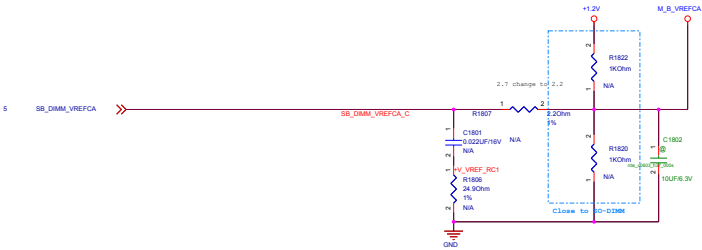
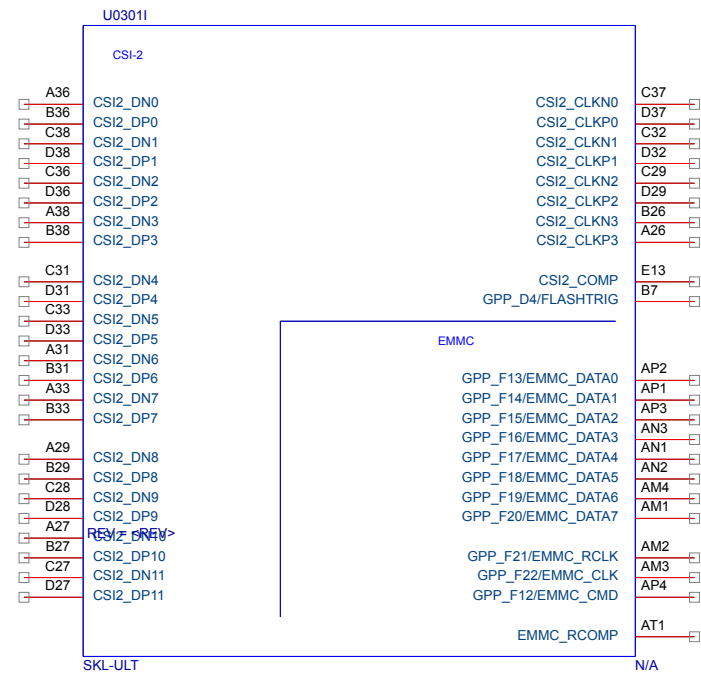


Figure 4-49. SKL U DDR4/-RS SODIMM V<sub>REF-CA</sub> Overview

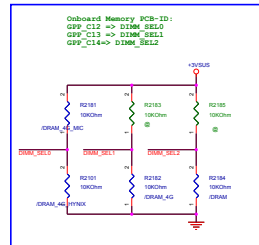
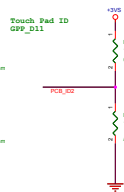
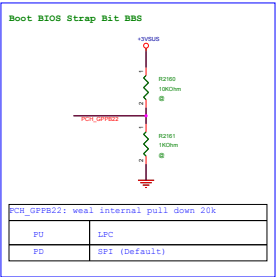


All Vref trace must be 20 mils width





## Main Board



DRAW Part Number		00000000000000000000	00000000000000000000
4G	00012-00010000	RVWIX/HSANAG0HAPP-PTC	0 0 0
	00012-00010300	RLCROB/WT40A512080B-083E1R	0 0 1
	00012-00030400	RVWIX/HSAN0G0HAPP-0MC	0 1 0
8G	00012-00030100	RLCROB/WT40A1080E-083E1R	0 1 1



# HD Audio

RN2201 near PCH

The diagram illustrates the HD Audio connections for the RN2201 component near the PCH. It includes a pin-to-pin connection table and a detailed RF requirement circuit diagram.

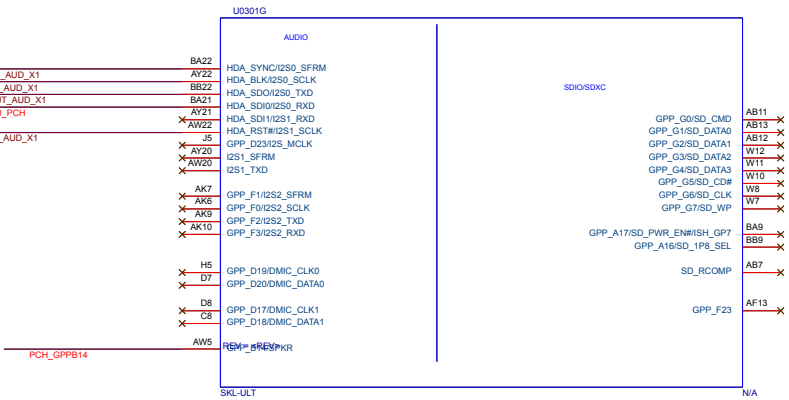
**Pin-to-Pin Connection Table:**

Pin	Signal	Pin	Signal	Pin	Signal
38	ACZ_BCLK_AUD	5	330HM	6	RN2201C
38	ACZ_SYNC_AUD	3	330HM	4	RN2201B
38	ACZ_RST#_AUD	1	330HM	NA	RN2201A
38	ACZ_SDOUT_AUD	7	330HM	NA	RN2201D
				NA	ACZ_RST#_AUD_X1
				NA	ACZ_SDOUT_AUD_X1

**RF Requirement Circuit Diagram:**

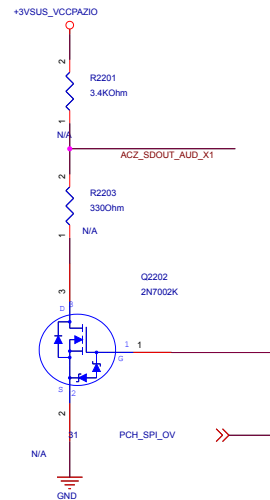
The RF requirement circuit diagram shows the connection of the ACZ\_BCLK\_AUD and ACZ\_SDINO\_AUD signals to the RN2201 component. The circuit includes two capacitors, C2201 and C2202, connected to the signals. The capacitors are connected to a 10PF/50V and 15PF/50V respectively. The ground connection is labeled GND.

**RF requirement**



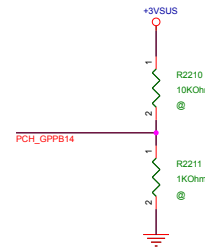
```
ACZ_SDOUT:(1) PCH: Internal PD 20k
ohm, VoLH =0.4V (2)
ALC3236:VIL<0.4xvddio, VIH>0.6xvddio
```

ACZ\_SDOUT is a signal used for Flash  
Descriptor security Override/ME debug mode  
HIGH : get overrideen, LOW : disable override--default



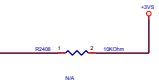
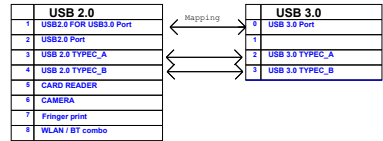
### Top-block Swap Override

**-block Swap Override**  
(invert an upper two 64-KB block address on access to SPI and FWH)

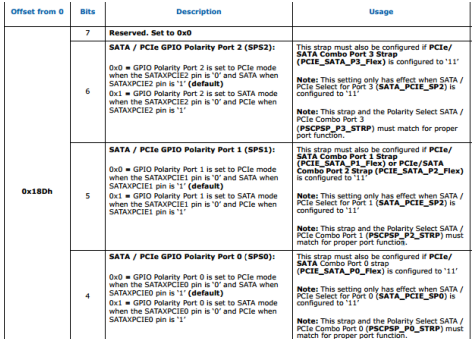


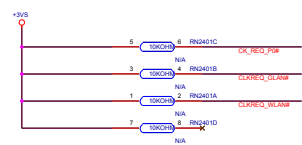
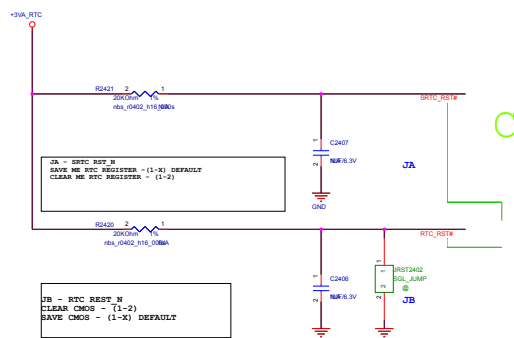
```
PCH_GPPB14: weak internal pull down
```

PU	Enable
PD	Disable top swap (default)



SATA PORT	SATA USAGE DEFAULT/OPTION
PORT 0	HDD
PORT 1	ODD
PORT 2	N/A
PORT 3	N/A

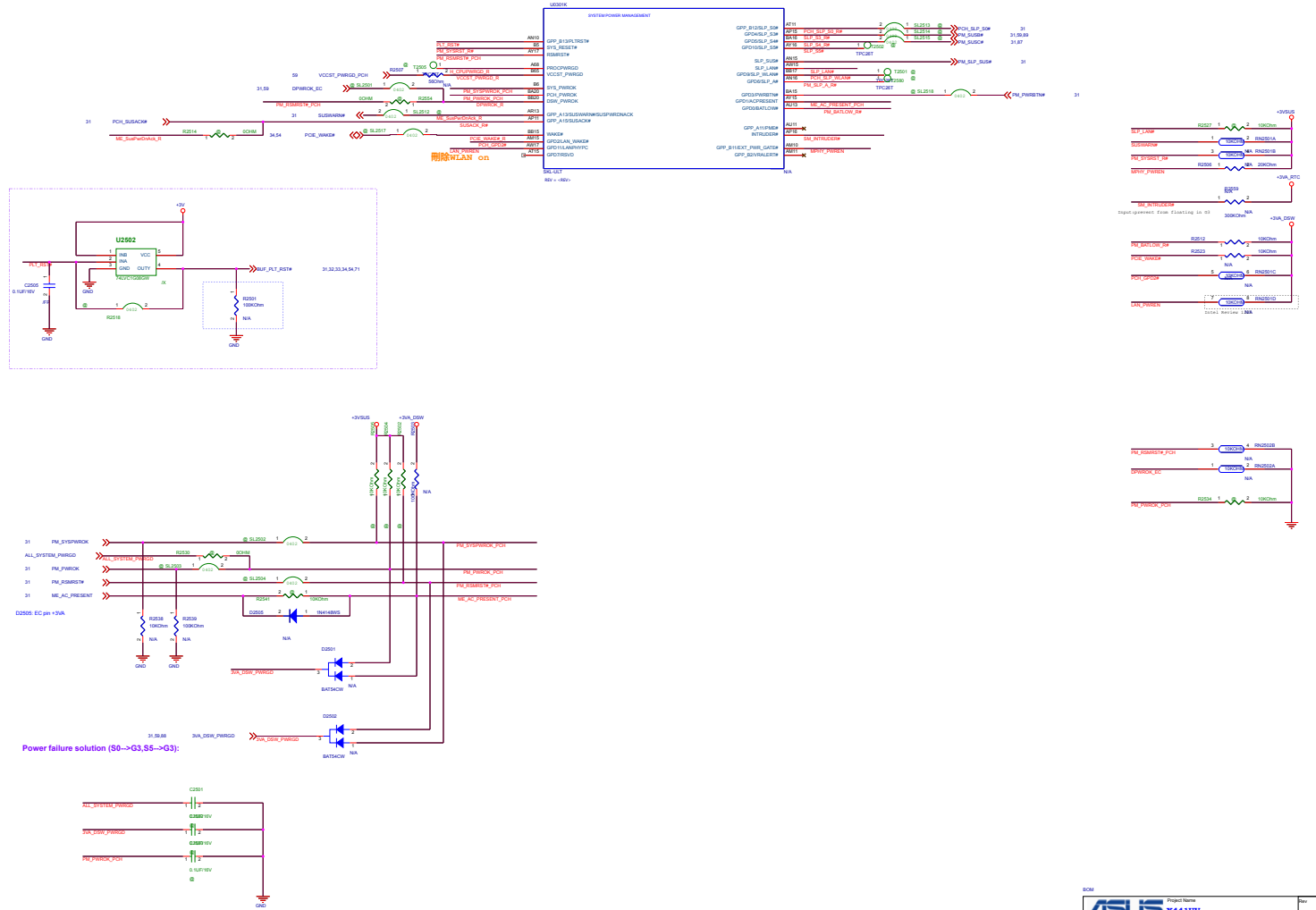


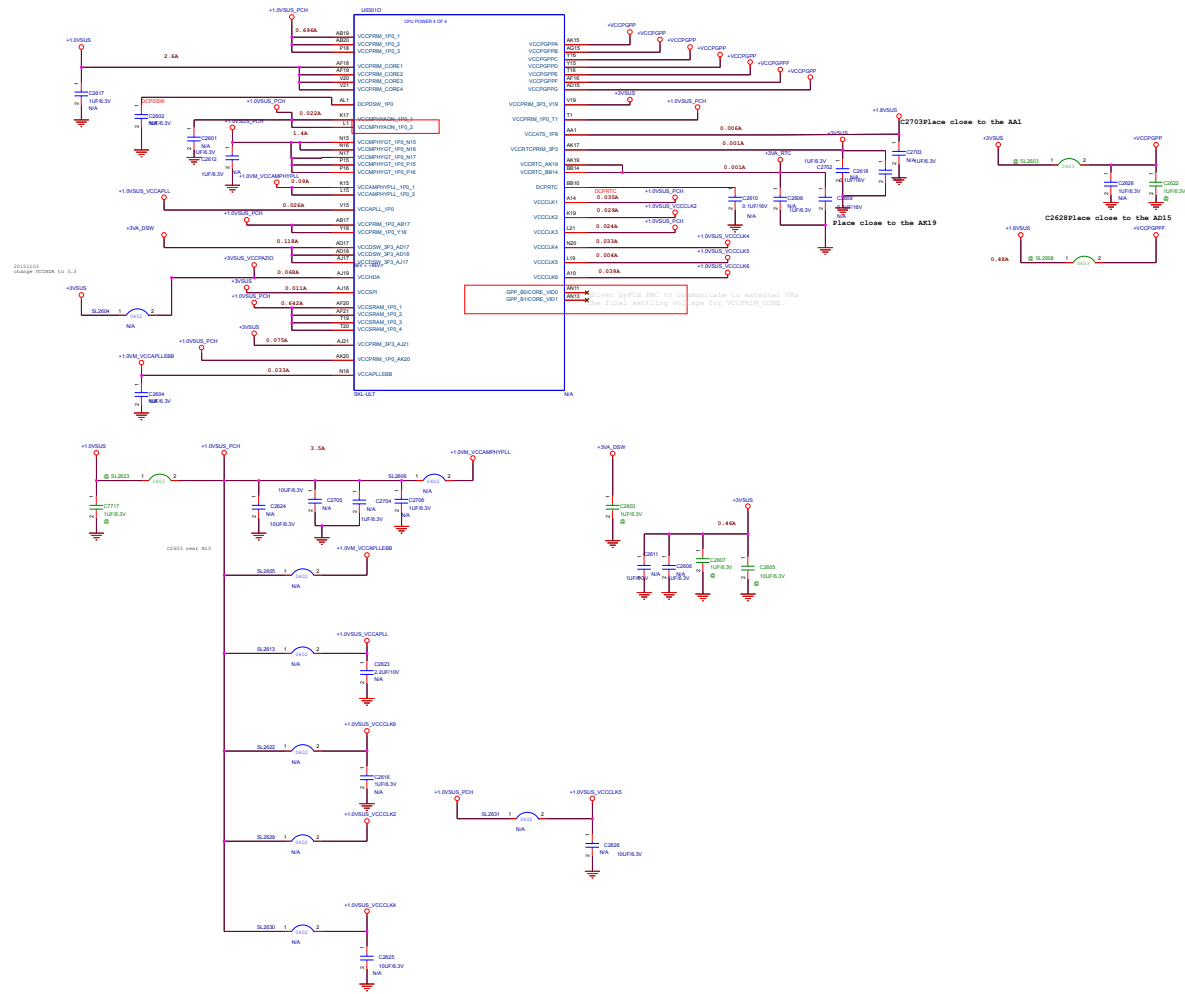
[illegible]

There must not  
be a jumper for SRTCRST# pin.

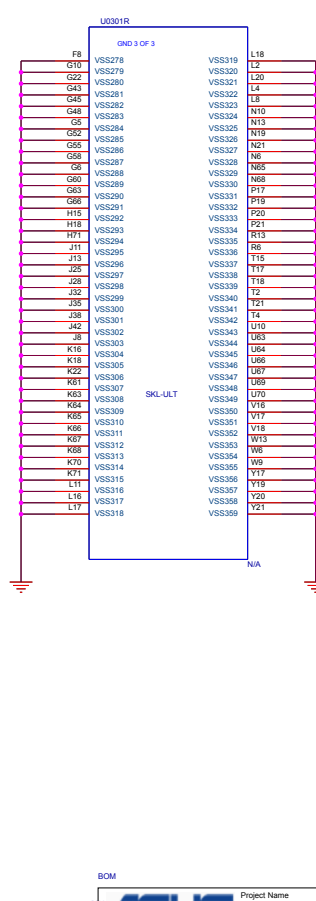
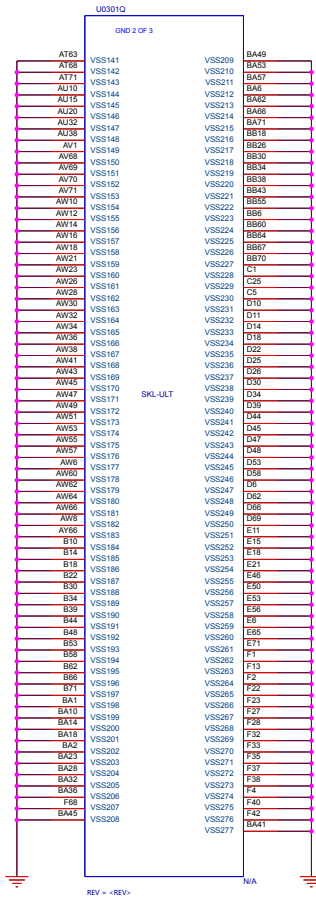
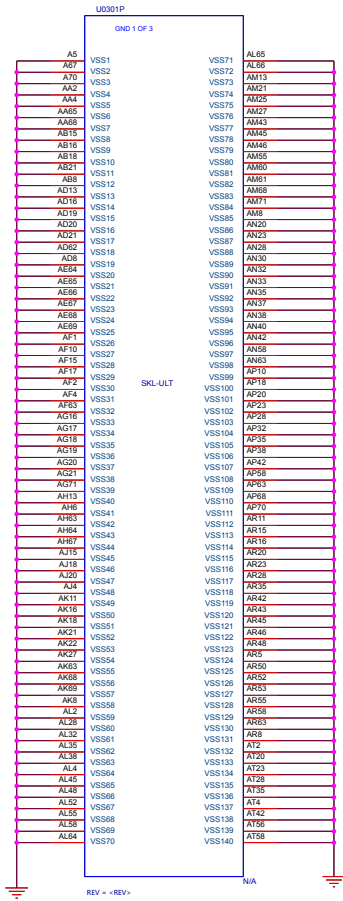


Main Board



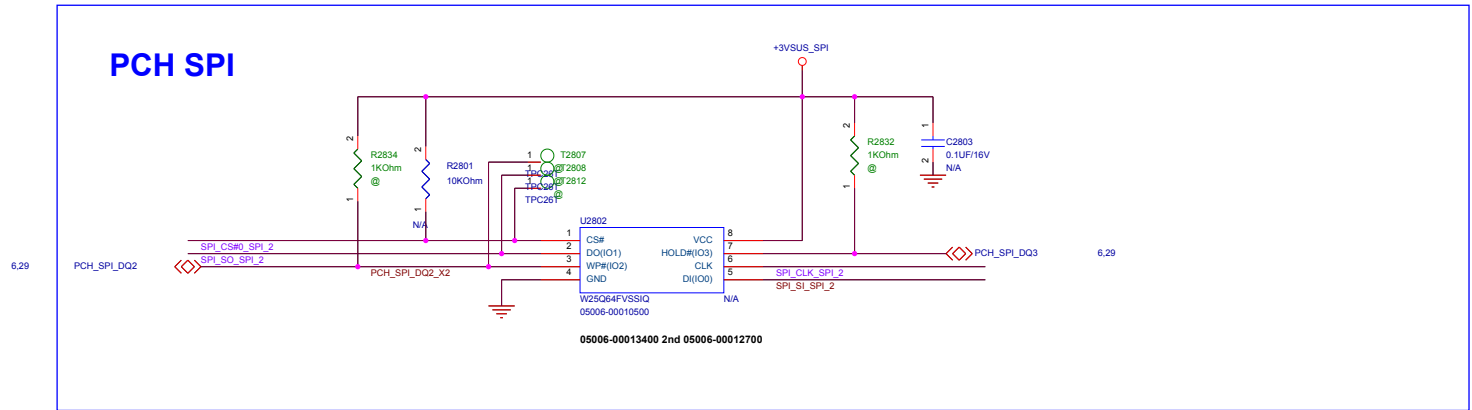
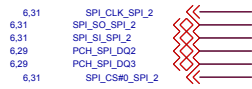
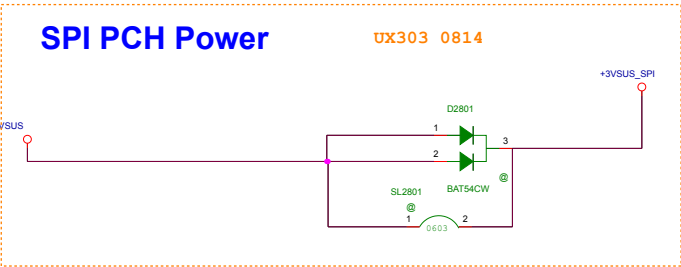


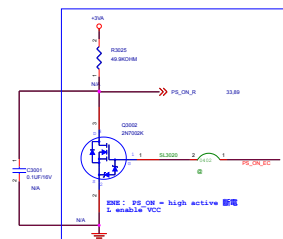
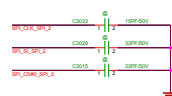
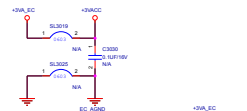
Doc#	Project Name	Rev
	<b>ASUS</b>	01.0
Title : GPU PCH Power and Ground		
Doc#	GPU PCH Power and Ground	01.0
Dep't	ASUS COMPUTER INC. Engineer: EE	
Date	2017-11-15	37 of 103



BOM

REV	ASUS	Project Name	Rev
		<b>X442</b>	R1.0
Title : CPU_PCH_POEWR_GND			
Size	Dept.: ASUSTek COMPUTER INC. Engineer: EE		
B	Date: Friday, October 13, 2017 Sheet 28 of 103		



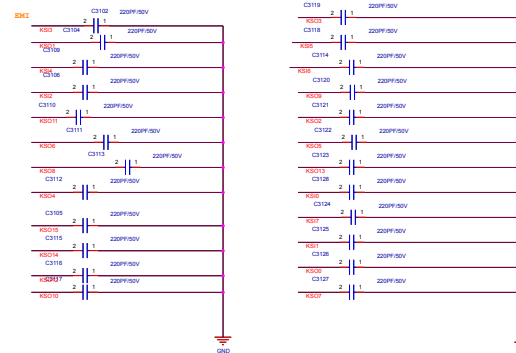


State	LPC	eSPI
902X	/non-eSPI	NA
903X	/non-eSPI /903X_non-eSPI	/eSPI

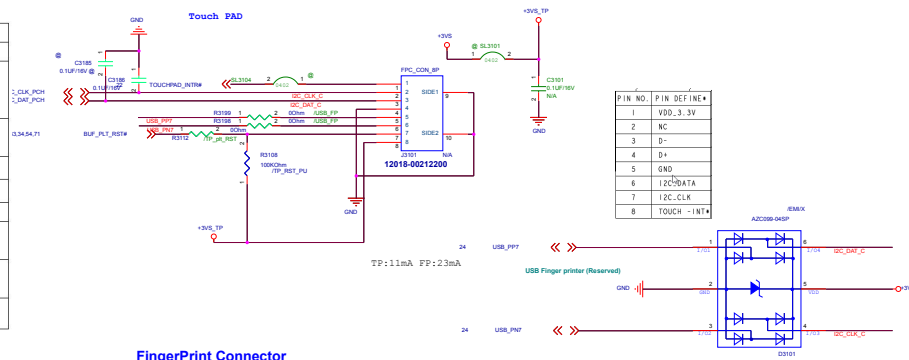


The schematic diagram illustrates the internal connections of the 12018-0020600 component. It features a central block labeled '12018-0020600' with various pins and internal components.

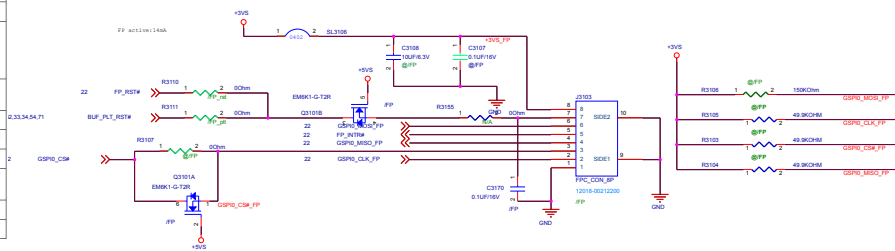
- Pin 1:** Labeled 'CEN101'.
- Pin 2:** Labeled 'END1'.
- Pin 27:** Labeled 'END2'.
- Pin 28:** Labeled 'END3'.
- Pin 29:** Labeled 'FAN\_CEN\_GND'.
- Pin 30:** Labeled 'GND'.
- Internal Components:**
  - A 'C3100 5.1UFH16V' capacitor is connected between pins 29 and 30.
  - A 'SE1008' component is connected between pins 27 and 28.
  - A 'PWR\_SSW' component is connected between pins 27 and 28.
- Internal Connections:**
  - Pin 1 is connected to a network of internal components including K3007, K3008, K3009, K3010, K3011, K3012, K3013, K3014, K3015, K3016, K3017, K3018, K3019, K3020, K3021, K3022, K3023, K3024, K3025, K3026, K3027, K3028, K3029, K3030, K3031, K3032, K3033, K3034, K3035, K3036, K3037, K3038, K3039, K3040, K3041, K3042, K3043, K3044, K3045, K3046, K3047, K3048, K3049, K3050, K3051, K3052, K3053, K3054, K3055, K3056, K3057, K3058, K3059, K3060, K3061, K3062, K3063, K3064, K3065, K3066, K3067, K3068, K3069, K3070, K3071, K3072, K3073, K3074, K3075, K3076, K3077, K3078, K3079, K3080, K3081, K3082, K3083, K3084, K3085, K3086, K3087, K3088, K3089, K3090, K3091, K3092, K3093, K3094, K3095, K3096, K3097, K3098, K3099, K3100, K3101, K3102, K3103, K3104, K3105, K3106, K3107, K3108, K3109, K3110, K3111, K3112, K3113, K3114, K3115, K3116, K3117, K3118, K3119, K3120, K3121, K3122, K3123, K3124, K3125, K3126, K3127, K3128, K3129, K3130, K3131, K3132, K3133, K3134, K3135, K3136, K3137, K3138, K3139, K3140, K3141, K3142, K3143, K3144, K3145, K3146, K3147, K3148, K3149, K3150, K3151, K3152, K3153, K3154, K3155, K3156, K3157, K3158, K3159, K3160, K3161, K3162, K3163, K3164, K3165, K3166, K3167, K3168, K3169, K3170, K3171, K3172, K3173, K3174, K3175, K3176, K3177, K3178, K3179, K3180, K3181, K3182, K3183, K3184, K3185, K3186, K3187, K3188, K3189, K3190, K3191, K3192, K3193, K3194, K3195, K3196, K3197, K3198, K3199, K3200, K3201, K3202, K3203, K3204, K3205, K3206, K3207, K3208, K3209, K3210, K3211, K3212, K3213, K3214, K3215, K3216, K3217, K3218, K3219, K3220, K3221, K3222, K3223, K3224, K3225, K3226, K3227, K3228, K3229, K3230, K3231, K3232, K3233, K3234, K3235, K3236, K3237, K3238, K3239, K3240, K3241, K3242, K3243, K3244, K3245, K3246, K3247, K3248, K3249, K3250, K3251, K3252, K3253, K3254, K3255, K3256, K3257, K3258, K3259, K3260, K3261, K3262, K3263, K3264, K3265, K3266, K3267, K3268, K3269, K3270, K3271, K3272, K3273, K3274, K3275, K3276, K3277, K3278, K3279, K3280, K3281, K3282, K3283, K3284, K3285, K3286, K3287, K3288, K3289, K3290, K3291, K3292, K3293, K3294, K3295, K3296, K3297, K3298, K3299, K3300, K3301, K3302, K3303, K3304, K3305, K3306, K3307, K3308, K3309, K3310, K3311, K3312, K3313, K3314, K3315, K3316, K3317, K3318, K3319, K3320, K3321, K3322, K3323, K3324, K3325, K3326, K3327, K3328, K3329, K3330, K3331, K3332, K3333, K3334, K3335, K3336, K3337, K3338, K3339, K3340, K3341, K3342, K3343, K3344, K3345, K3346, K3347, K3348, K3349, K3350, K3351, K3352, K3353, K3354, K3355, K3356, K3357, K3358, K3359, K3360, K3361, K3362, K3363, K3364, K3365, K3366, K3367, K3368, K3369, K3370, K3371, K3372, K3373, K3374, K3375, K3376, K3377, K3378, K3379, K3380, K3381, K3382, K3383, K3384, K3385, K3386, K3387, K3388, K3389, K3390, K3391, K3392, K3393, K3394, K3395, K3396, K3397, K3398, K3399, K3400, K3401, K3402, K3403, K3404, K3405, K3406, K3407, K3408, K3409, K3410, K3411, K3412, K3413, K3414, K3415, K3416, K3417, K3418, K3419, K3420, K3421, K3422, K3423, K3424, K3425, K3426, K3427, K3428, K3429, K3430, K3431, K3432, K3433, K3434, K3435, K3436, K3437, K3438, K3439, K3440, K3441, K3442, K3443, K3444, K3445, K3446, K3447, K3448, K3449, K3450, K3451, K3452, K3453, K3454, K3455, K3456, K3457, K3458, K3459, K3460, K3461, K3462, K3463, K3464, K3465, K3466, K3467, K3468, K3469, K3470, K3471, K3472, K3473, K3474, K3475, K3476, K3477, K3478, K3479, K3480, K3481, K3482, K3483, K3484, K3485, K3486, K3487, K3488, K3489, K3490, K3491, K3492, K3493, K3494, K3495, K3496, K3497, K3498, K3499, K3500, K3501, K3502, K3503, K3504, K3505, K3506, K3507, K3508, K3509, K3510, K3511, K3512, K3513, K3514, K3515, K3516, K3517, K3518, K3519, K3520, K3521, K3522, K3523, K3524, K3525, K3526, K3527, K3528, K3529, K3530, K3531, K3532, K3533, K3534, K3535, K3536, K3537, K3538, K3539, K3540, K3541, K3542, K3543, K3544, K3545, K3546, K3547, K3548, K3549, K3550, K3551, K3552, K3553, K3554, K3555, K3556, K3557, K3558, K3559, K3560, K3561, K3562, K3563, K3564, K3565, K3566, K3567, K3568, K3569, K3570, K3571, K3572, K3573, K3574, K3575, K3576, K3577, K3578, K3579, K3580, K3581, K3582, K3583, K3584, K3585, K3586, K3587, K3588, K3589, K3590, K3591, K3592, K3593, K3594, K3595, K3596, K3597, K3598, K3599, K3600, K3601, K3602, K3603, K3604, K3605, K3606, K3607, K3608, K3609, K3610, K3611, K3612, K3613, K3614, K3615, K3616, K3617, K3618, K3619, K3620, K3621, K3622, K3623, K3624, K3625, K3626, K3627, K3628, K3629, K363



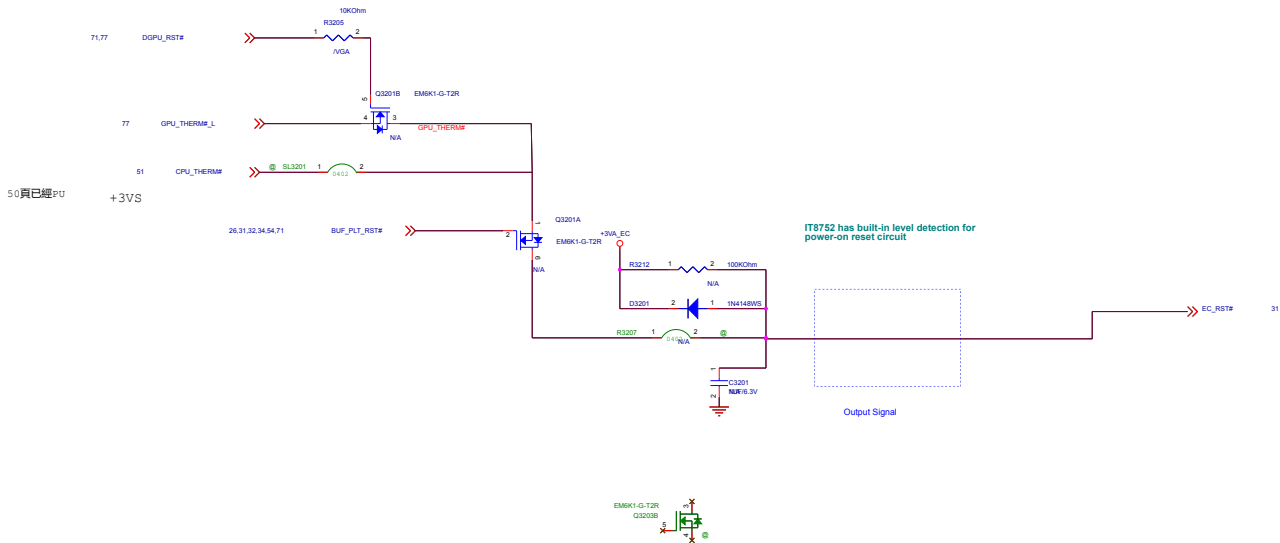
connector type: 8 pins FFC connector, pitch is 0.5 mm.



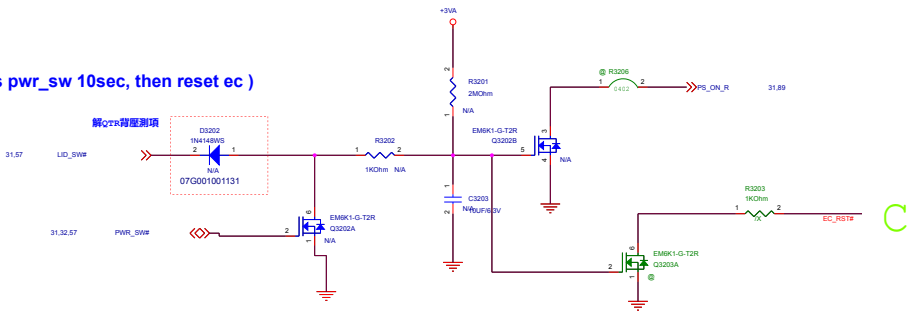
injector type: 8 pins FFC connector, pitch is 0.5 mm.



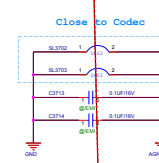
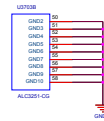
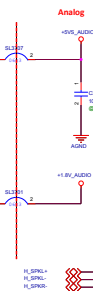
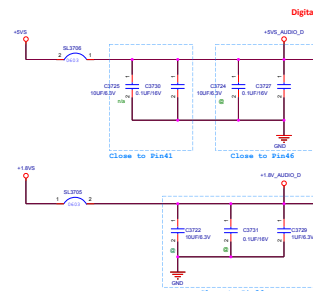
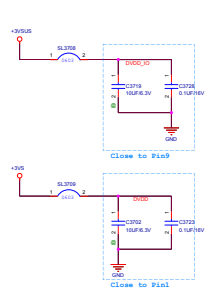
Thermal Policy



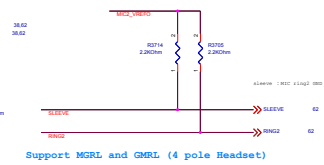
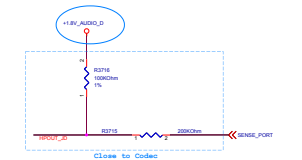
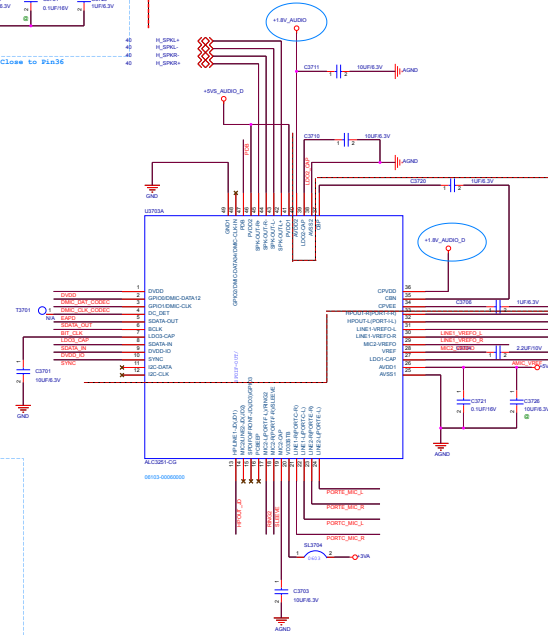
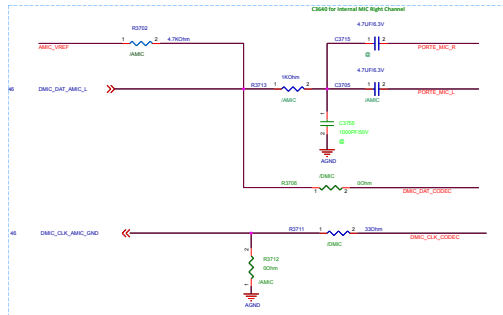
battery embedded (press pwr\_sw 10sec, then reset ec )



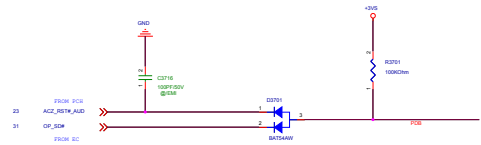
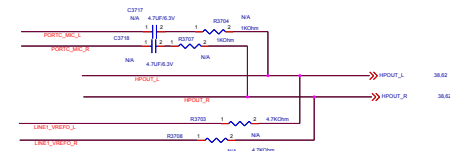


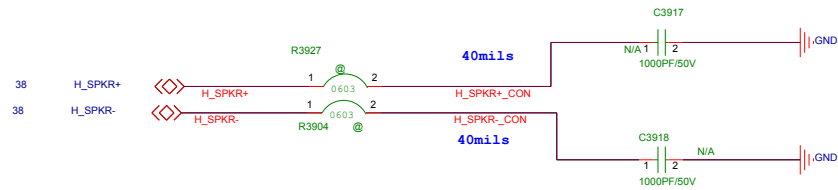


Internal Analog MIC & Array Mic (reserve)

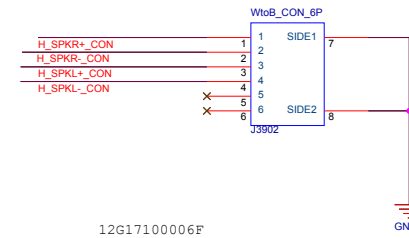
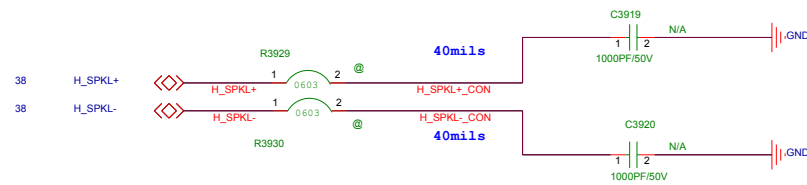


SLEEVE/RING2 至少走線40mil, 越短越好



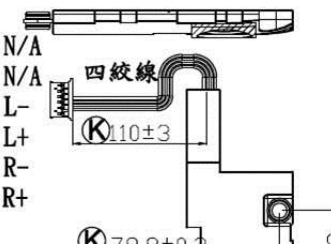


Speaker = 1.5W 7.20hm per Channel

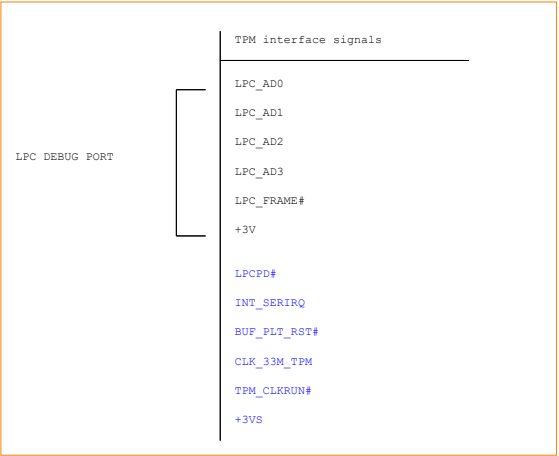
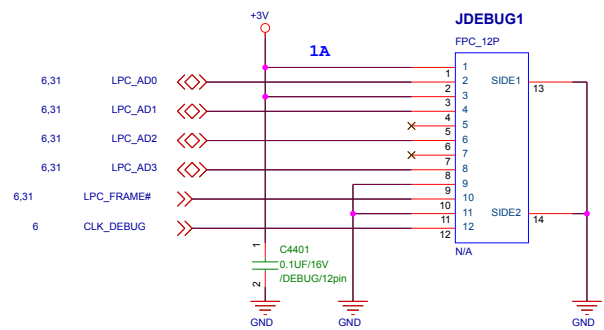


94 V-2)

- |   |       |     |
|---|-------|-----|
| 6 | BLACK | N/A |
| 5 | BLACK | N/A |
| 4 | WHITE | L-  |
| 3 | BLUE  | L+  |
| 2 | BLACK | R-  |
| 1 | RED   | R+  |



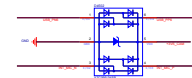
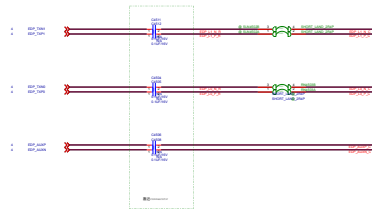
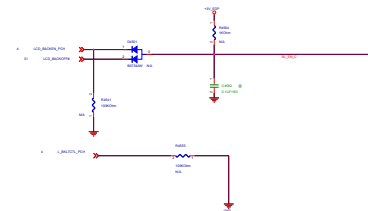
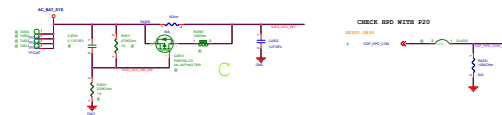
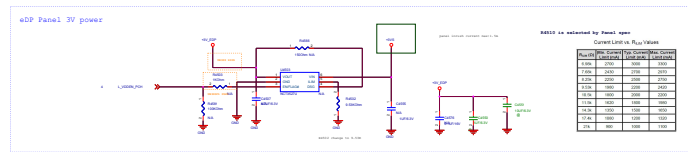
LPC DEBUG PORT



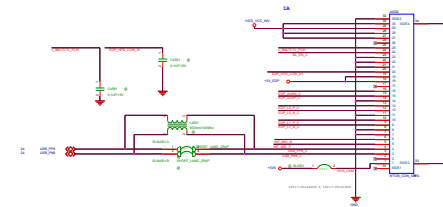
BOM

<b>ASUS</b>		Project Name	Rev
		<b>X441UV</b>	R1.0
Title : <b>DEBUG PORT</b>			
Size	Dept.: <b>ASUSTeK COMPUTER INC.</b> Engineer: <b>EE</b>		
A			
Date: Friday, October 13, 2017	Sheet	45	of 103

eDP Panel

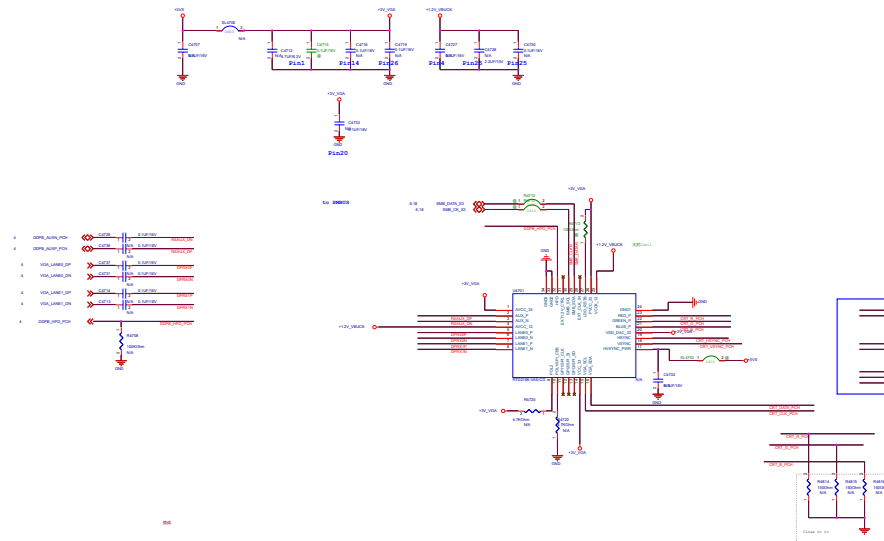


eDP CONNECTOR



The diagram illustrates a 16-to-1 multiplexer architecture. It features 16 data inputs (D0-D15) and 4 select inputs (S0-S3). The inputs are connected to a network of 16 multiplexers (M0-M15) in a hierarchical structure. The outputs of these multiplexers are connected to a final 16-to-1 multiplexer (M16) which produces the output Y. The diagram is color-coded: green for select inputs, blue for data inputs, and red for control signals. The output Y is shown as a single line.

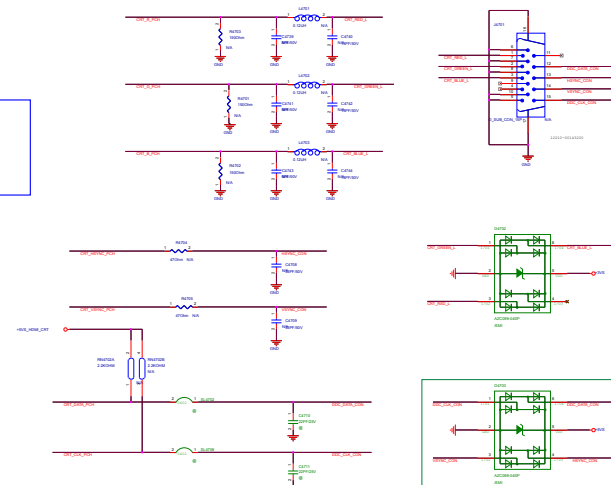
eDP to VGA



LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

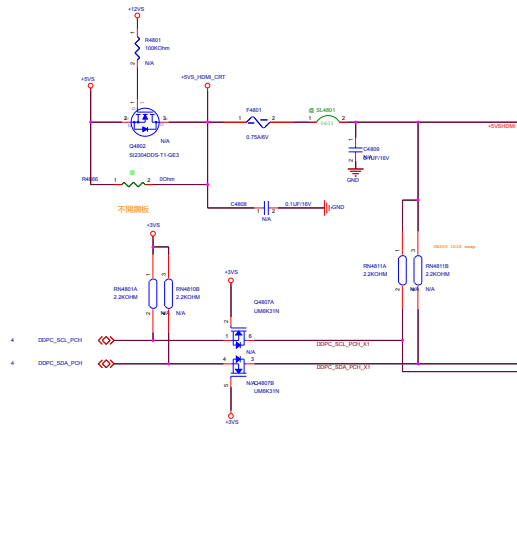
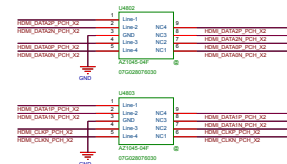
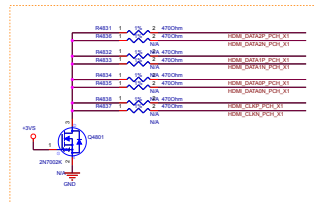
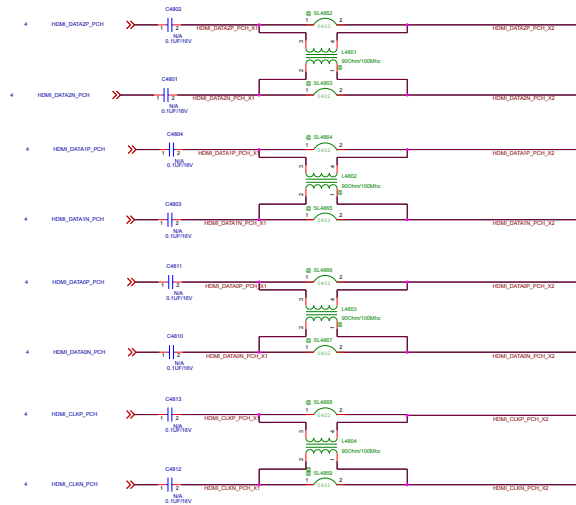
		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

CRT D-SUB

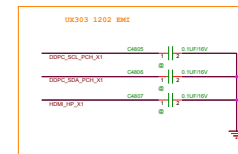
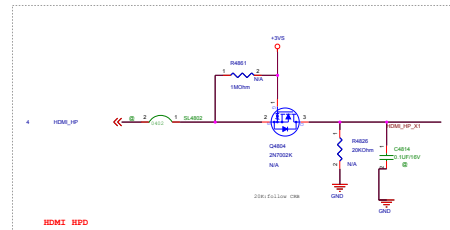




Close to CONNECTOR  
Near CON J4801



M : 12022-00092900

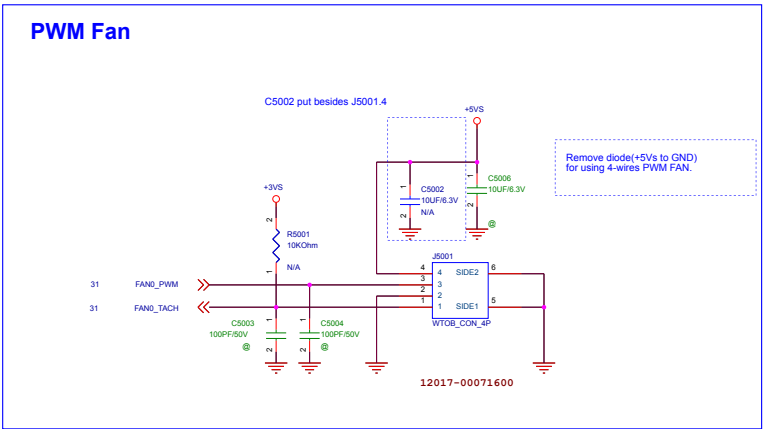


BCM	Project Name	Rev
	X4410V	01.0
Title :	HDMI-type D	
Dept. :	ASUSTEK COMPUTER INC. Engineer: EE	
Date: Friday, October 10, 2017	Page 49 of 100	

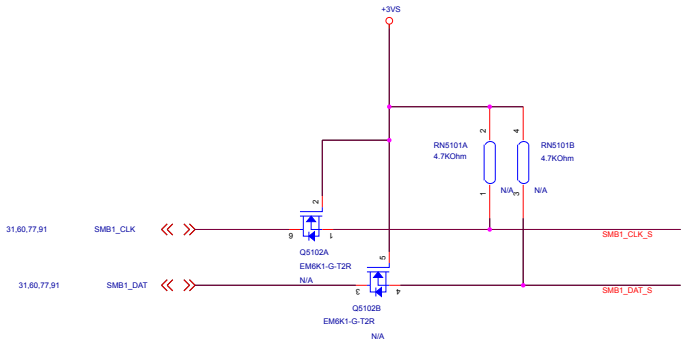
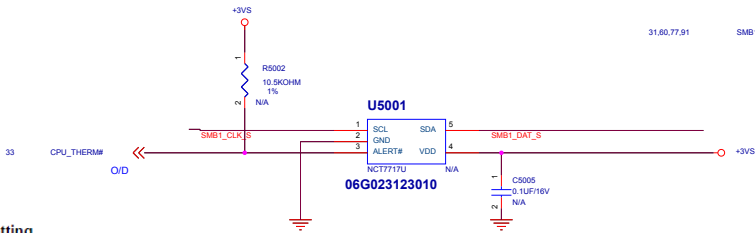
## GPU Thermal Sensor

Tung, 0302-6 Add GPU Thermal Sensor (P50)

### PWM Fan



### CPU Thermal Sensor



#### 5.3 Address Setting

NCT7771U I2C/SMBus address is 1001000xb (x is R/W bit).

#### 5.6 ALERT# point hardware power-on setting (TBD)

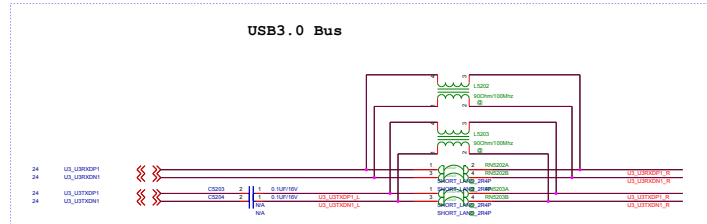
The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin :

PULL-UP RESISTOR		TEMPERATURE (°C)
ALERT	2KΩ	75
	7.5KΩ	90
	10.5KΩ	100
	14KΩ	105
	18.7KΩ	110

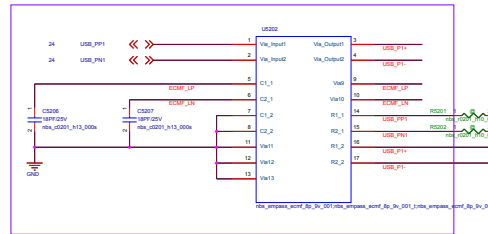
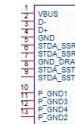
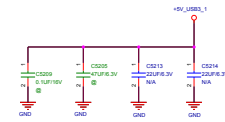
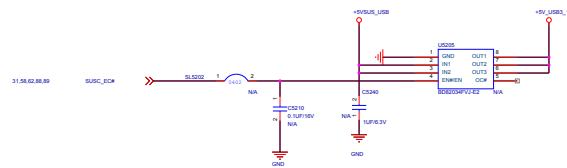
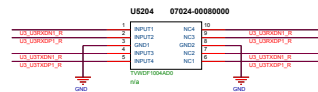
Route CPU\_THRM\_DA , CPU\_THRM\_DC and on the same layer

-----OTHER SIGNALS  
10 mils  
=====GND  
10 mils  
=====H\_THERMDA(10 mils)  
10 mils  
=====H\_THERMDC(10 mils)  
10 mils  
=====GND  
10 mils  
-----OTHER SIGNALS  
Avoid FSB,Power

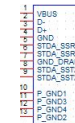
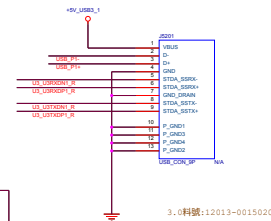
## USB 3.0 con.



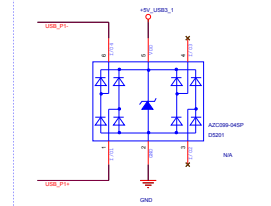
### USB3.0 ESD-Protection



USB2.0 EMI-Protection With ECMP (PCB 1.2 & 1.0mm\_8Layer)

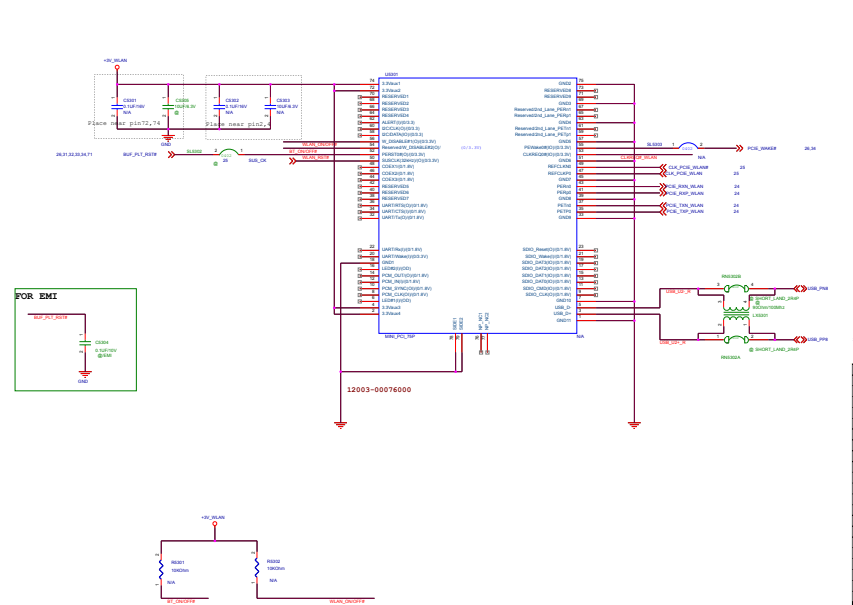
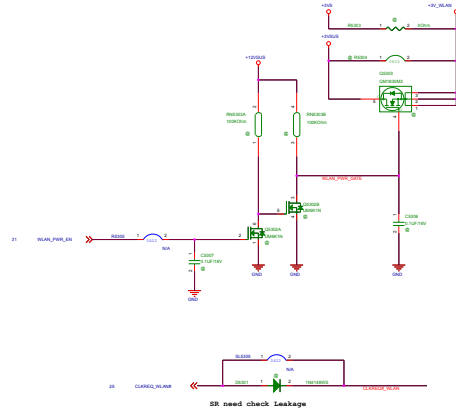


### USB2.0 ESD-Protection



2.0 料號: 12012-00063900  
12012-00063900

## NGFF KEY E con.

[illegible]

VBUS Power	CC Pull Up (4.75-5.5V)	CC Pull Up (3.3V +/- 5%)
Default USB Power	56k Ohm +/-20%	36k Ohm +/-20%
1.5A @ 5V	22k Ohm +/-5%	12k Ohm +/-5%
3.0A @ 5V	10k Ohm +/-5%	4.7k Ohm +/-5%

CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

[illegible]

USB 2.0

C.M. choke 有負向問題 !!

24 USB\_PN3 24 USB\_PP3

100nF

100pF

1000 turns

B=1.1

L=500nH

R=0.000107

USBP\_A\_C USBP\_B\_C

[illegible]

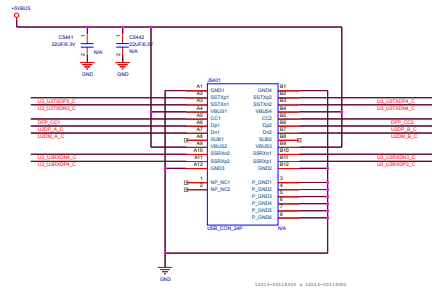
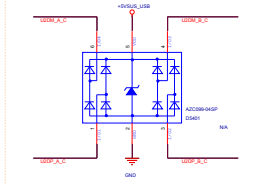
NOTE: 走線請直接由 U0901 穿過緊零件另一側之對pin, 勿分成枝狀走線

NOTE: 走線請直接由 U0901 穿過至零件另一側之對應pin, 勿成分枝狀走線

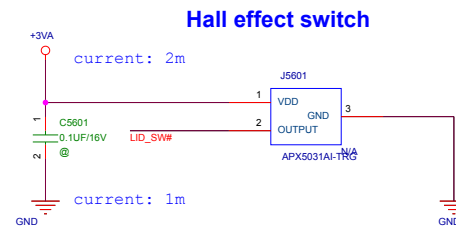
NOTE: 走線請直接由 U0901 穿過緊零件另一側之對準 pin，勿分成枝狀走線

NOTE: 走線請直接由 U0901 穿過至零件另一側之對應pin, 勿成分枝狀走線

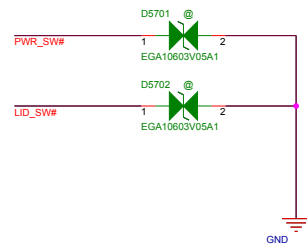
ESD chip should be 5V tolerance



12013-00116300 a 12013-00119300

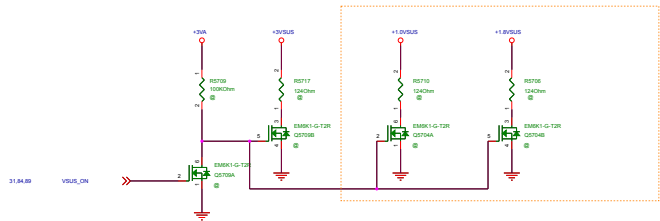
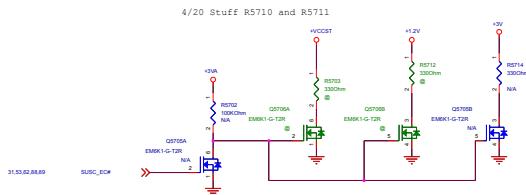
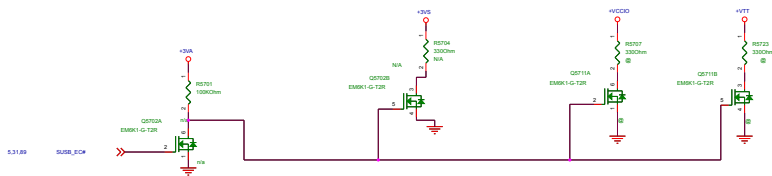


06033-00140000

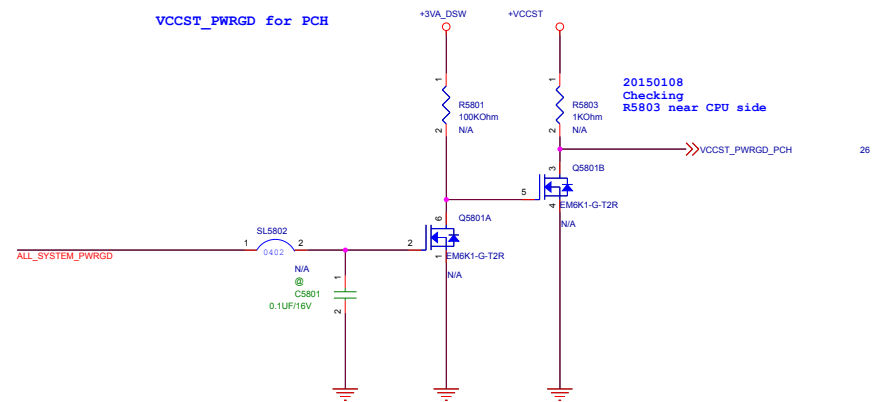
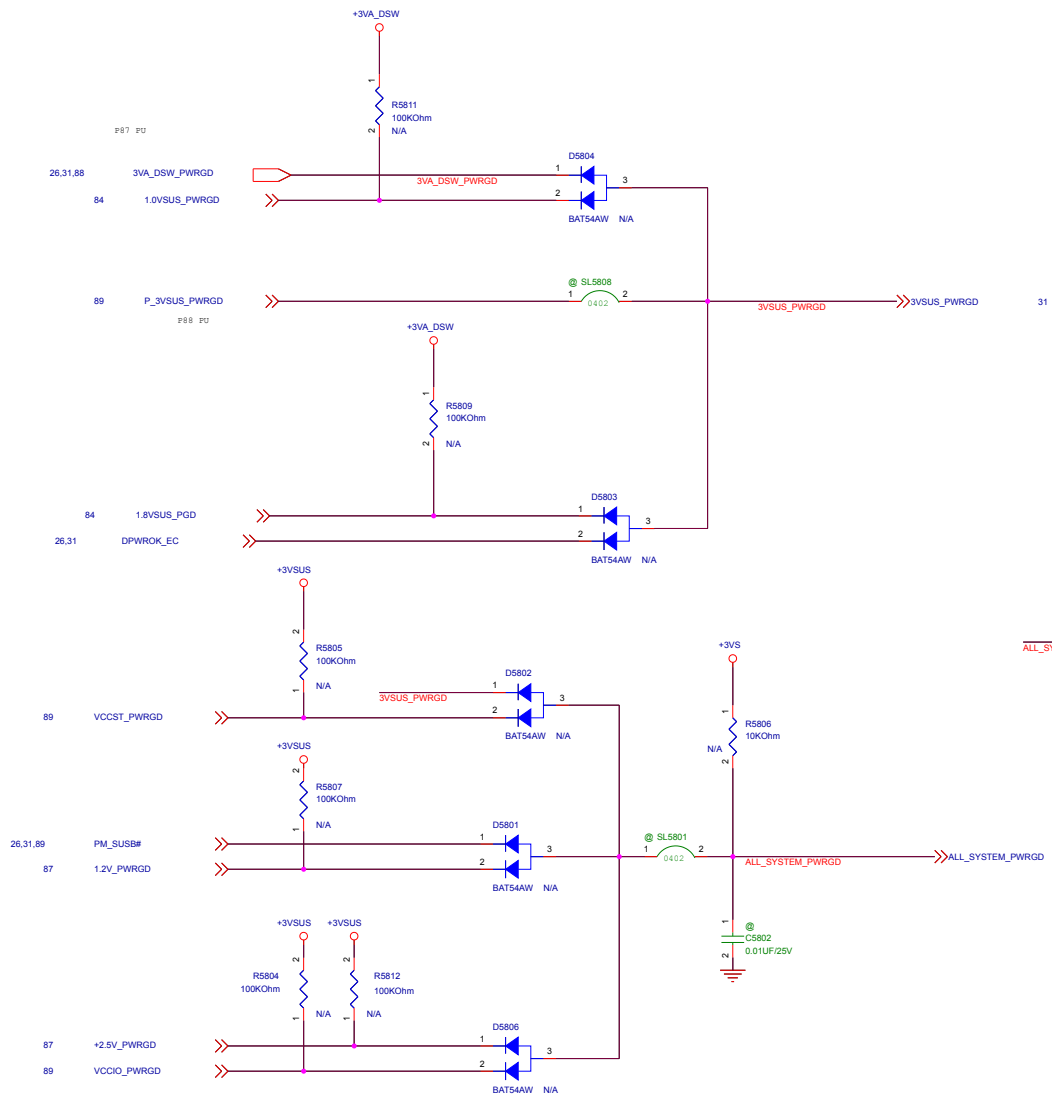


ASUS X441		Project Name	Rev
Title : PWR_SW&HALL_SW			R1.0
Size	Dept.: ASUSTeK COMPUTER INC. Engineer: EE		
A			
Date: Friday, October 13, 2017	Sheet	57	of 103

Main Board



BCM	Project Name	Rev
	ASUS X441UV	R1.0
Title : DSG Discharge		
Date	Dept.: ASUS COMPUTER INC. Engineer: EE	
Date: Friday, October 13, 2017	Drawn: 88	of 103



BOM

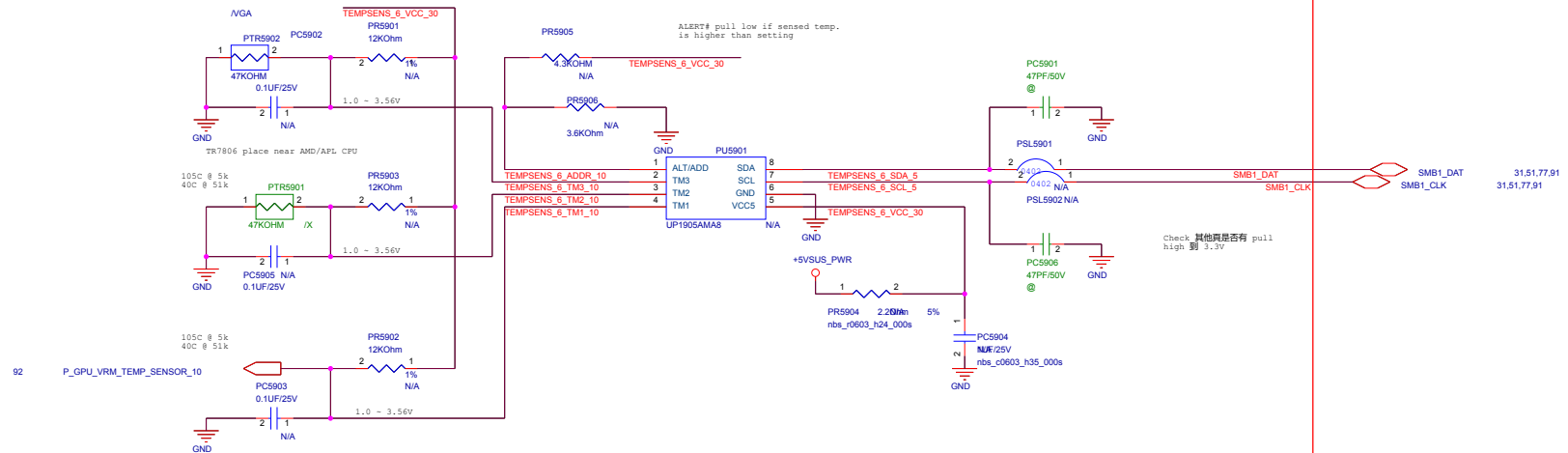
<b>ASUS</b>		Project Name	Rev
		<b>X441UV</b>	R1.0
<b>Title : PRO_Protect</b>			
Size	Dept.: ASUStek COMPUTER INC. Engineer: EE		
B	Date: Friday, October 13, 2017		
		Sheet	59 of 103



Address Selection Table

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
R78012	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
R78113	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

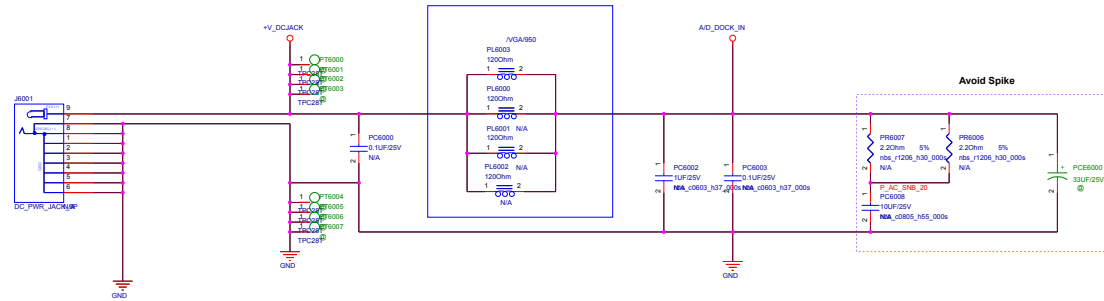
TR7807 place near VRAM ,  
SSD base on thermal RD test



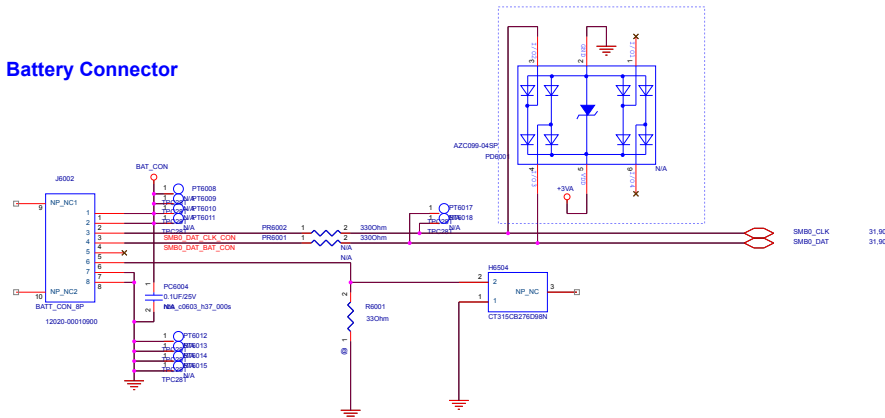
BOM

<b>ASUS</b>		Project Name	Rev
<b>X442</b>			R1.0
Title : NGFF_WWAN			
Size	Dept.:	ASUSTek COMPUTER INC.	Engineer: EE
B			
Date: Friday, October 13, 2017	Sheet	60	of 103

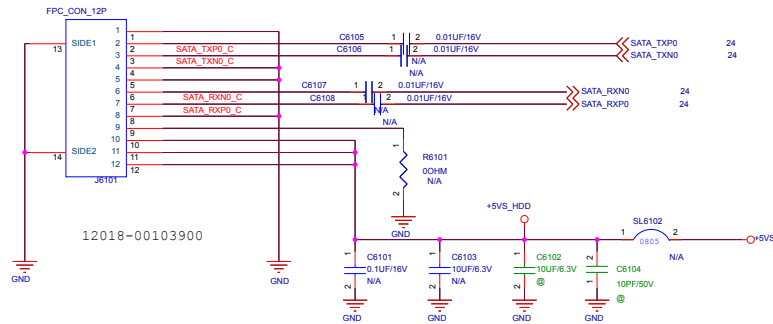
0603 Bead rule:  
33W: Bead\*2;  
45W, 65W : bead\* 3;  
90W, 120W, 150W: Bead\*4;  
180W, 230W: bead\*6



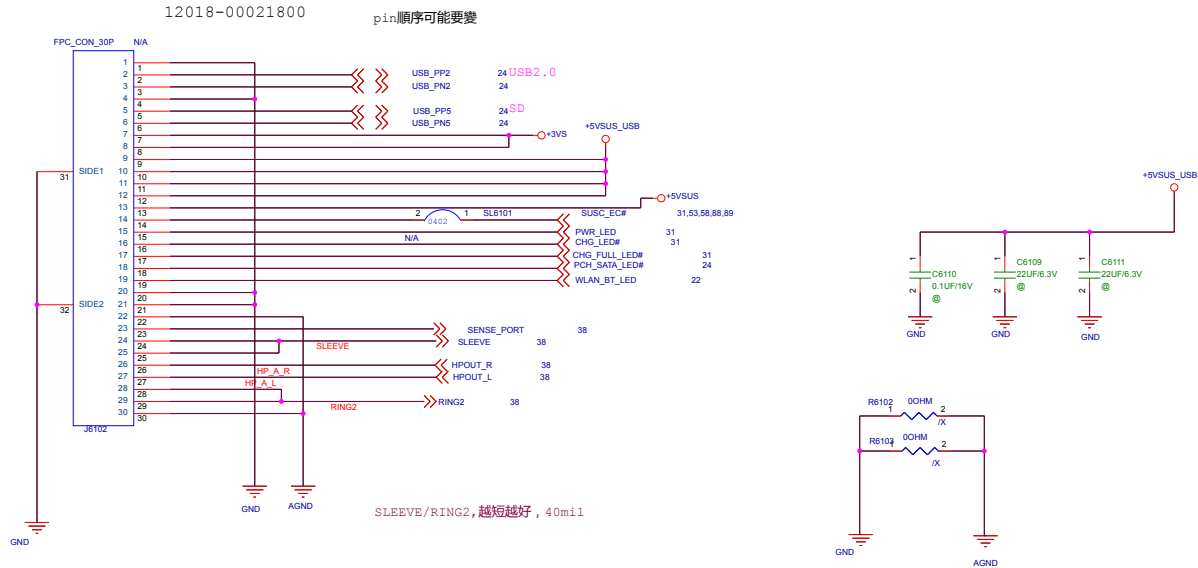
## Battery Connector



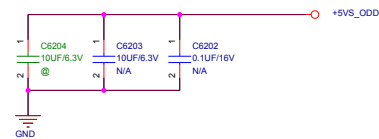
HDD BD FPC CONNECTOR

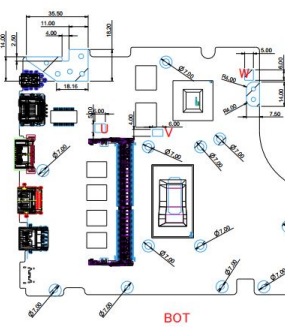
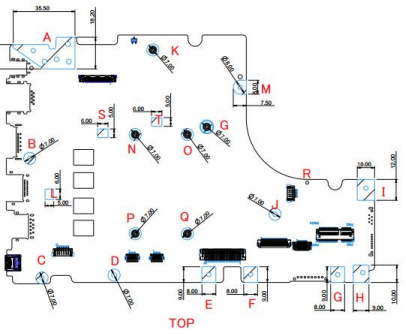
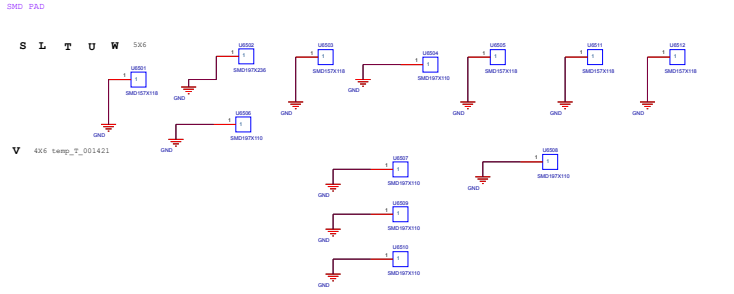
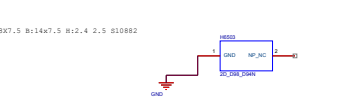
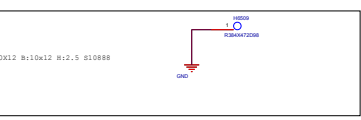
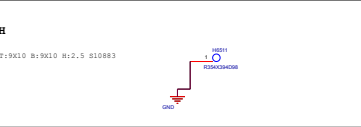
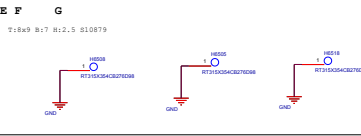
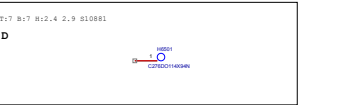
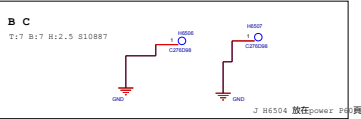
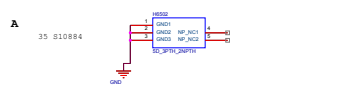
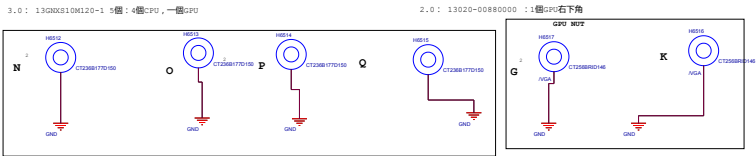


IO BD FPC CONNECTOR(SD+U2.0+AudioJack+LED)



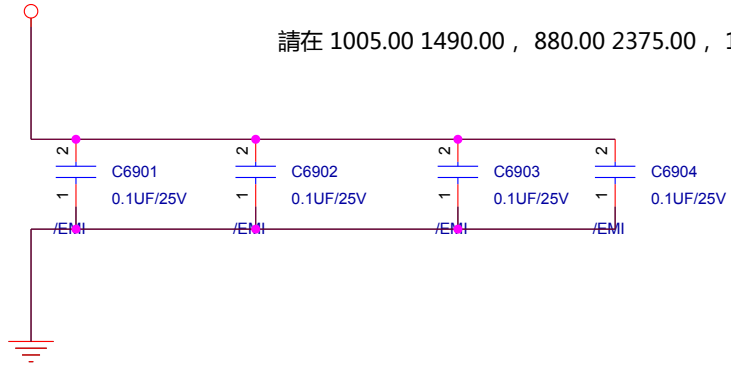
BOM		Project Name	
ASUS		x442U	
Title :		Sensors	
Size	Dept.:	ASUSTek COMPUTER INC.	Engineer: EE
B			
Date: Friday, October 13, 2017		Sheet	62 of 103





AC\_BAT\_SYS

請在 1005.00 1490.00 , 880.00 2375.00 , 1075.00 3340.00 , 3255.00 3375.00附近預留 AC\_BAT\_SYS對gnd的 0.1uf電容

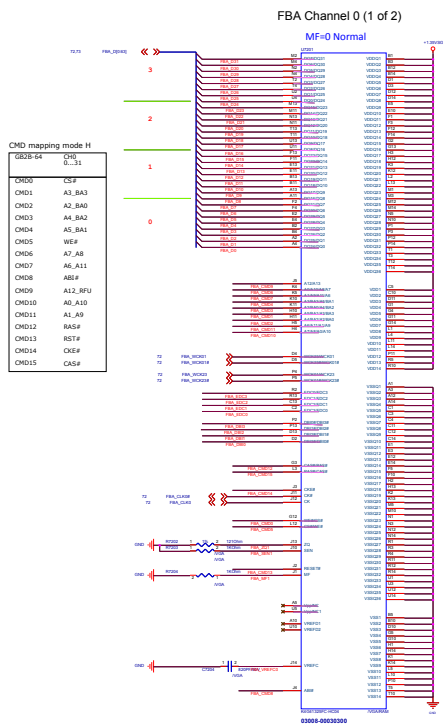
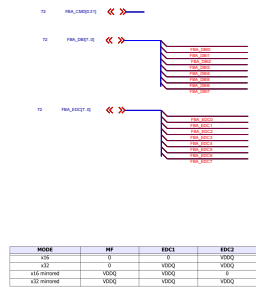




 Project Name <b>X442</b>		Rev R1.0
<b>Title :</b> N14M-GE_PCIE		
Size Custom	<b>Dept.:</b> ASUS14M COMPUTER INC. <b>Engineer:</b> EE	
Date: Friday, October 13, 2017		Sheet 71 of 103

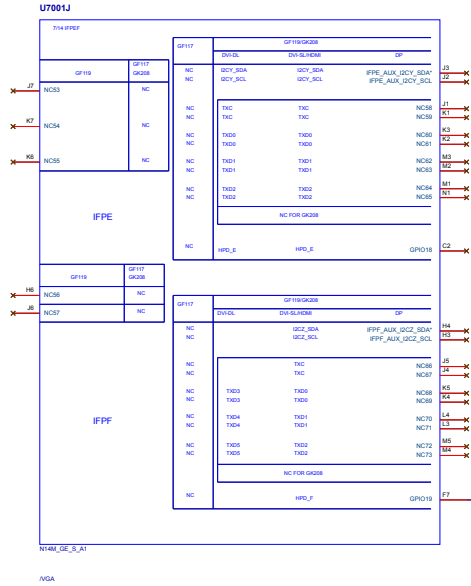
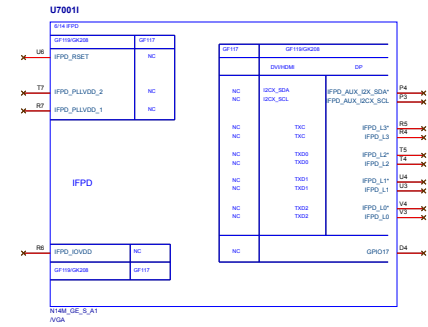
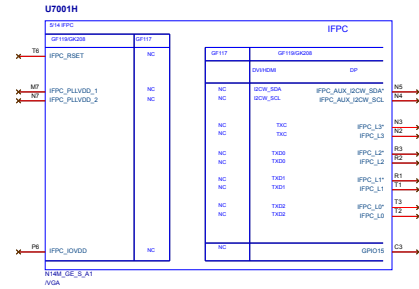
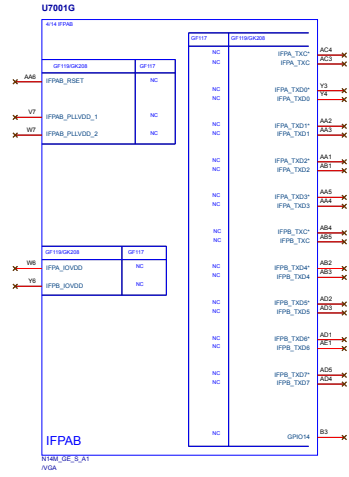




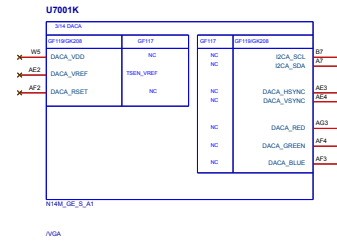


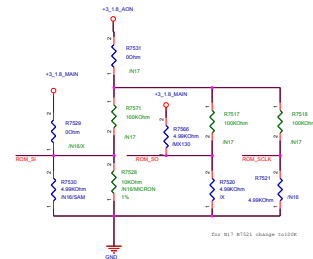
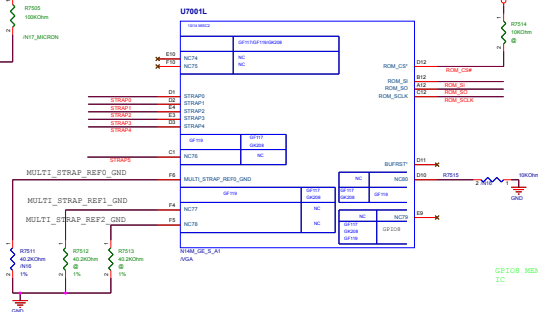
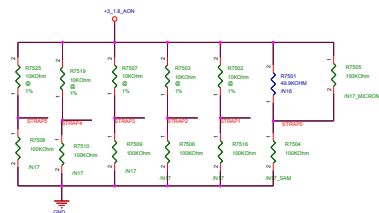


## LVDS



CRT

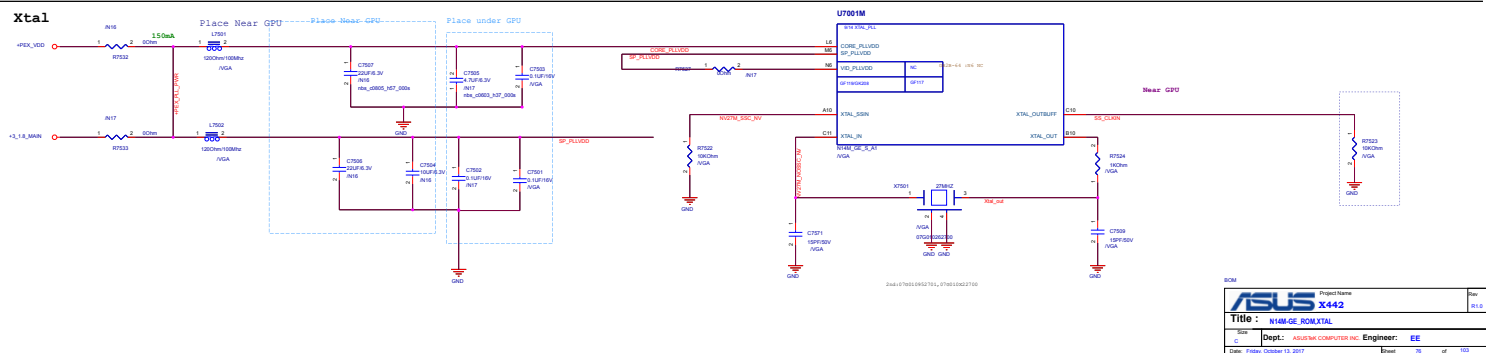




GPIO8 MEM\_VDD\_CTLGPD0 = 1.35VSG power IC

4.99 k = 1.00212449914010  
24.9 k = 1.00212449914010  
45.3k = 1.00212453214010

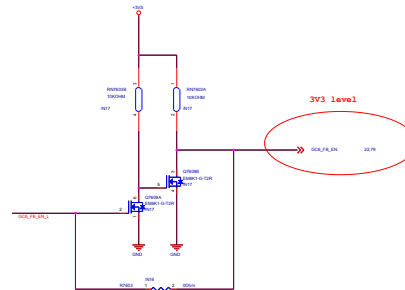
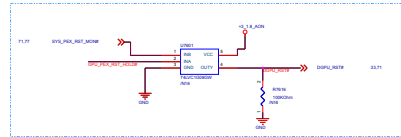
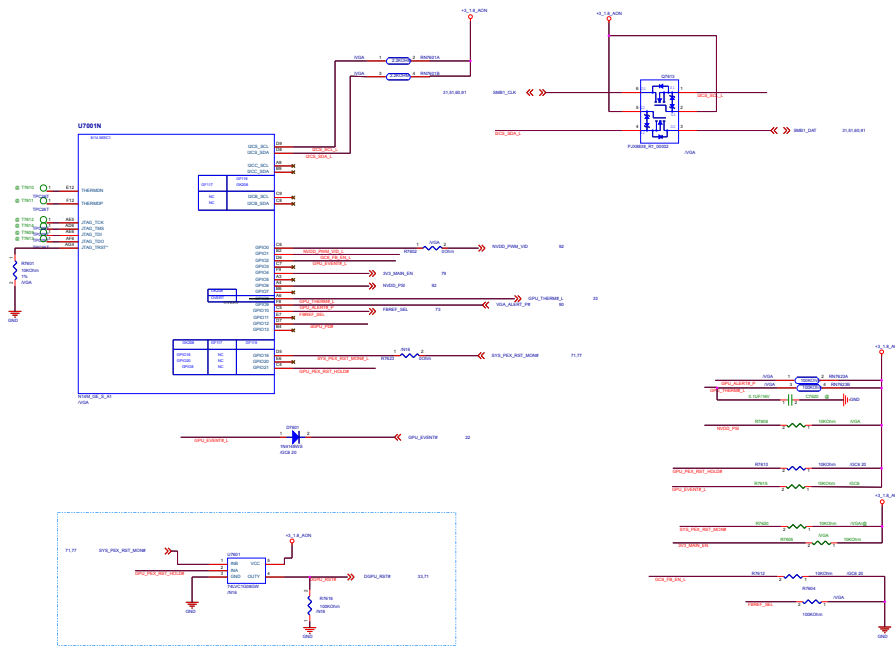
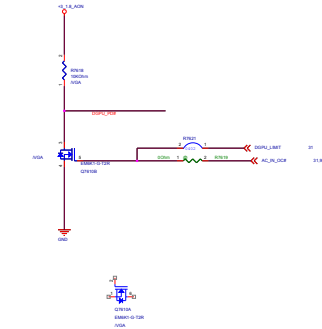
PN	Type/Config	VRAM	RAM_CFG	IS
03008-000304000	000R5 128M*32 28 1.5V FBGA170	ELPD4EDW4032BAG-60.F	0x4	PD 24.9
03008-000313000	000R5 128M*32 28 1.5V FBGA170	SAMSUNGK4G41325FE-HC2B	0x7	PD 45.3K
03008-000503000	000R5 256M*32 6.0 1.5V FBGA170	MICRONMT51J256M32HF-60.A	0x1	PD 15K
03008-000501100	000R5 256M*32 6.0 1.5V FBGA170	SAMSUNGK4G80325F-B-HC03	0x0	PD 4.99K



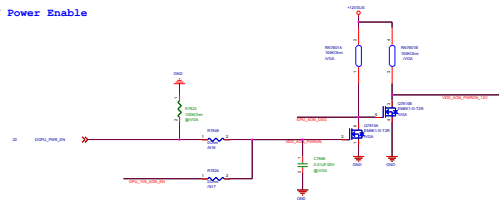
ASUS	Project Name	Rev
		01.0
Title :	R/W:GE, R/W:XTAL	
Dept :	ASUS INC. COMPUTER INC.	Engineer: EE
Date:	Friday, October 12, 2012	Drawn: EE

Table 10. N16/GB2B-64 and N17/GB2C-64 GPIO Differences

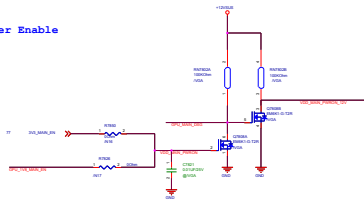
GPIO Pin	N16 GPU Function	N14 GPU Function on Co-Design	N17 GPU Function	Comments
GPIO0	GCA_FB_EN	PWM_VID	PWM_VID	N17 PWM_VID for NVVIDEO supply
GPIO1	MDA_VDD_CTL	GCA_FB_EN	GCA_FB_EN	
GPIO2	LCD_BL_PWM	GPU_EVENT#	GPU_EVENT#	
GPIO3	LCD_VCC	NVVIDEO_PWM	NVVIDEO_PWM	N17 PWM_VID for NVVIDEO supply
GPIO4	LCD_BLEN	3V3_MAN_EN	3V3_MAN_EN	
GPIO5	3V3_MAN_EN	FRAME_LOCK#	FRAME_LOCK#	
GPIO6	GPU_EVENT#	PSI	PSI	(342 PS for NVVIDEO supply)
GPIO7	3D_VISION	LCD_BL_PWM	LCD_BL_PWM	
GPIO8	3V3_PCL_RST_HOLD#	FFF_HPD	MDA_VDD_CTL	
GPIO9	THERM_ALERT	THERM_ALERT	THERM_ALERT	Same
GPIO10	MDA_VREF_CTL	MDA_VREF_CTL	MDA_VREF_CTL	Same
GPIO11	PWM_VID	LCD_VDD	LCD_VDD	
GPIO12	PWM_LEVEL	PWM_LEVEL	PWM_LEVEL	Same
GPIO13	PSI	LCD_BLEN	LCD_BLEN	
GPIO14	HPD_FPA	HPD_FPA	HPD_FPA	Same
GPIO15	HPD_FPC	HPD_FPC	HPD_FPC	
GPIO16	FRAME_LOCK#	3V3_PCL_RST_HOLD#	RESERVED	
GPIO17	HPD_FPD	HPD_FPD	HPD_FPD	Same
GPIO18	HPD_FPE	HPD_FPE	HPD_FPE	Same
GPIO19	HPD_FPF & HPD_FPS	3D_VISION	3D_VISION	
GPIO20	RESERVED	FFC_FPD	RESERVED	
GPIO21	GPU_BEL_RST_HOLD#	GPU_RST_HOLD#	RESERVED	
GPIO22	RESERVED	RESERVED	RESERVED	New N17 GPIO
GPIO23	RESERVED	RESERVED	RESERVED	New N17 GPIO



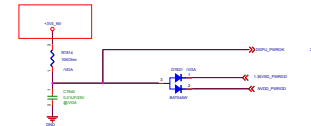
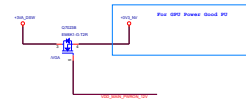
### +3\_1\_8\_AON Power Enable



### +3\_1\_8\_MAIN Power Enable



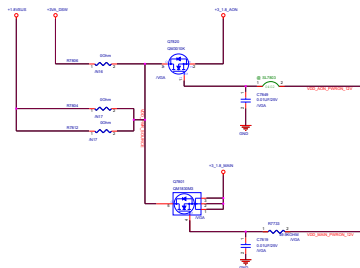
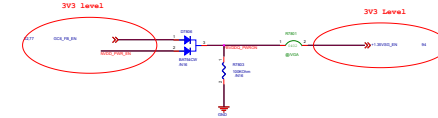
### GPU POWER GOOD



### NVDD Power Enable



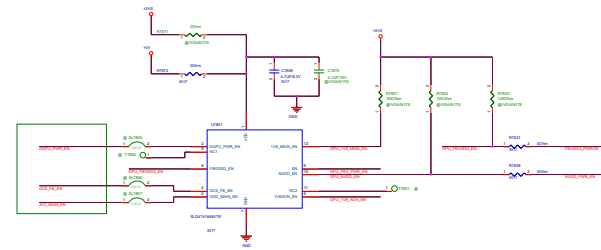
### FBVDDQ Power Enable



### N17S GPU Sequence Solution

#### Input Signal for N17S

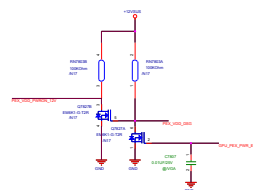
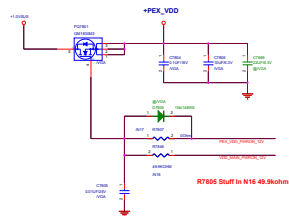
1. GPU1\_PWR\_EN(3.3V)
2. GPU1\_PWR\_EN(3.3V)
3. GPU1\_PWR\_EN(3.3V)
4. GPU1\_PWR\_EN(3.3V)



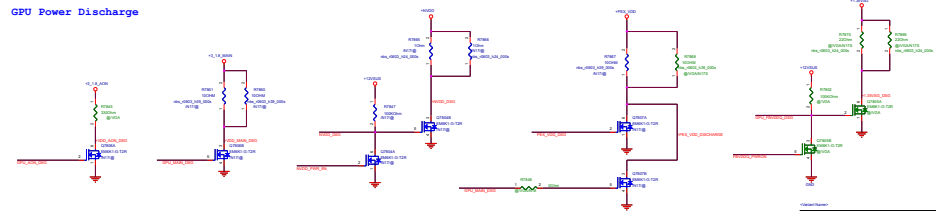
#### Output Signal for N17S(3.3V)

1. GPU1\_PWR\_EN(3.3V)
2. GPU1\_PWR\_EN(3.3V)
3. GPU1\_PWR\_EN(3.3V)
4. GPU1\_PWR\_EN(3.3V)

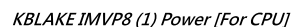
### PEX\_VDD Power Enable



### GPU Power Discharge



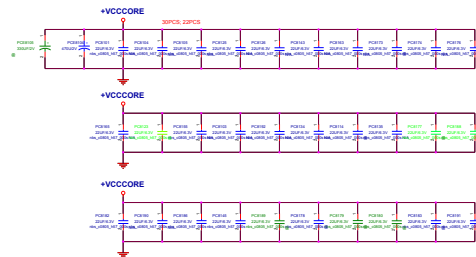
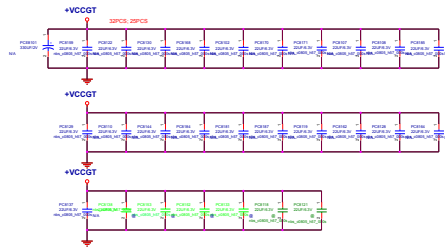
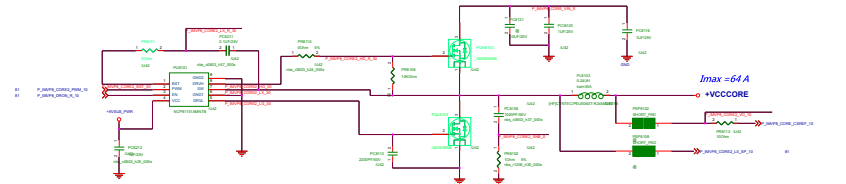
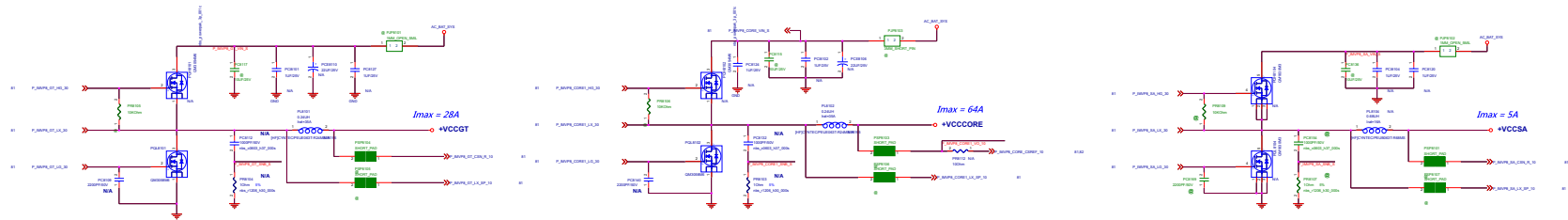
Q704 Q705 Q707 BOM Stuff in 0705-0202000



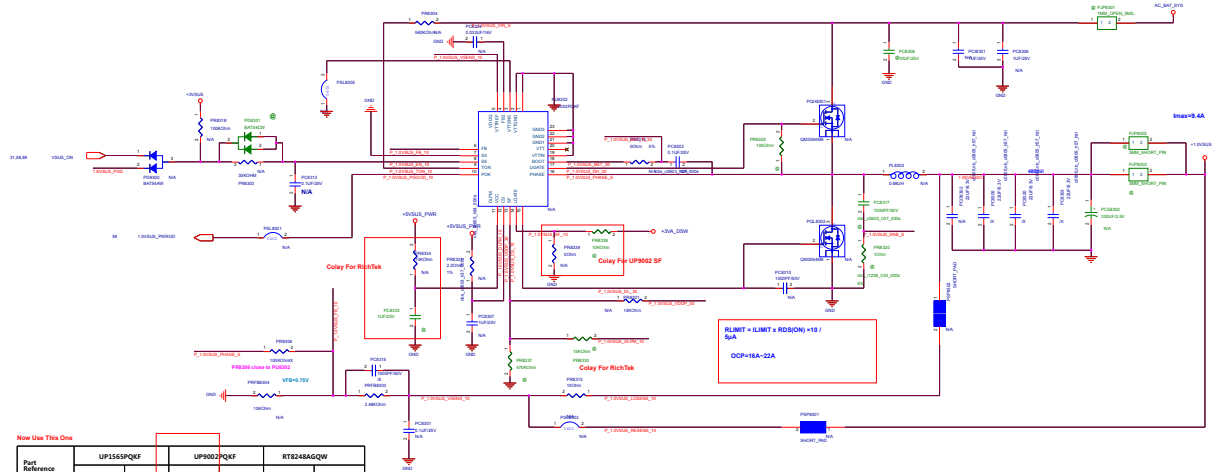
U42/U22 BOM optional

ASUS		Project Name		S	
		UX510		P	
Title : SPIW, KBLAKE, U42, U22, IMVP5					
Size		Dept: AGIS Power Team		Engineer: Power	
Date: Friday, October 19, 2007		Email		del not 100	

# Kaby Lake-U IMVP8 Power (2) [For CPU]



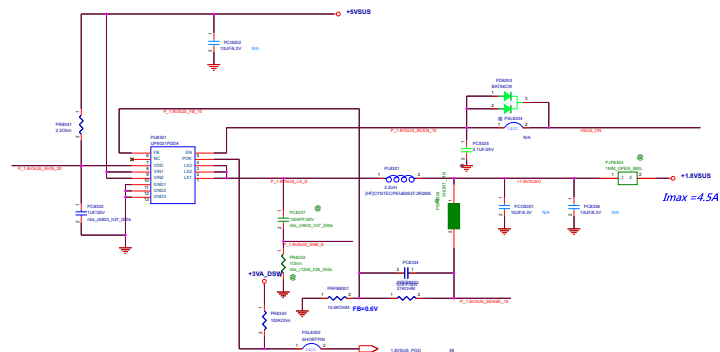
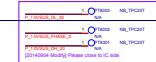




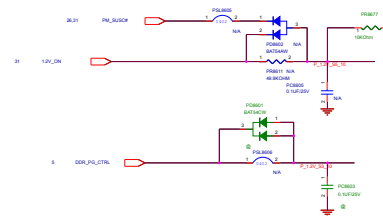
Now Use This One

Part Reference	UP556PQJF		UP9002PQJF		RT8248AGQW	
	MLCC	V-CHIP	MLCC	V-CHIP	MLCC	V-CHIP
988334	2.2uohm	2.2uohm	100uohm	100uohm	⊗	⊗
PC8333	1uF	1uF	⊗	⊗	0ohm	0ohm
988327	⊗	⊗	3000uohm	3000uohm		
988304	8200uohm	8200uohm	5600uohm	5600uohm	8200uohm	8200uohm
988306	1700uohm	4020uohm	1000uohm	⊗	1.700uohm	⊗
PC8315	820pF	820pF	1000pF	⊗	820pF	⊗
988301	150uohm	150uohm	150uohm	150uohm	⊗	⊗
988330	⊗	⊗	⊗	⊗	150uohm	150uohm

+1.8VSUS [For PCH]

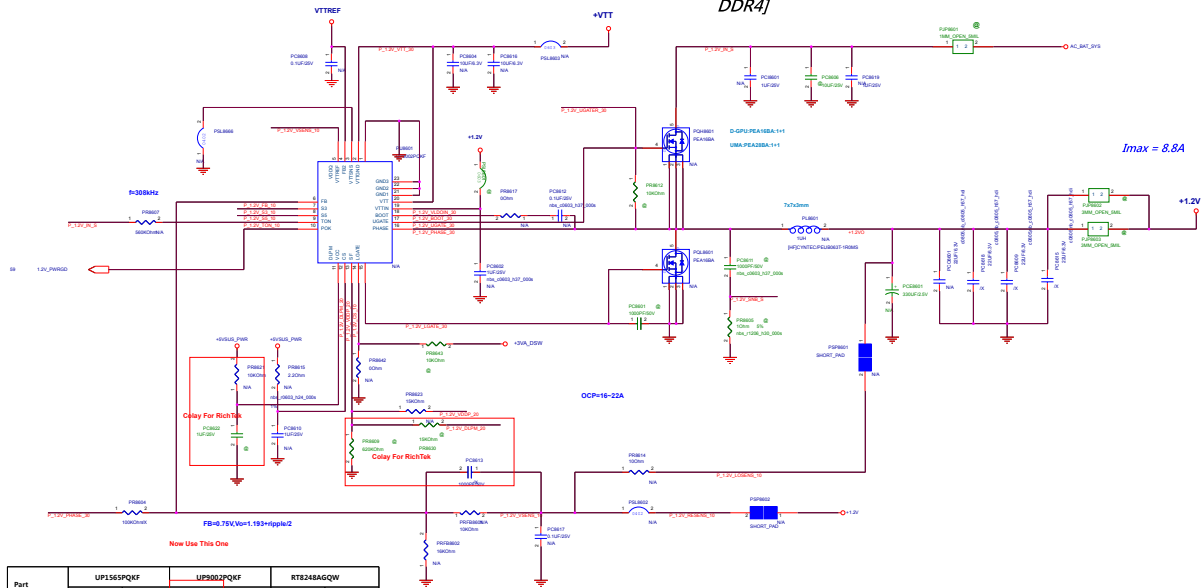


$I_{max} = 4.5A$

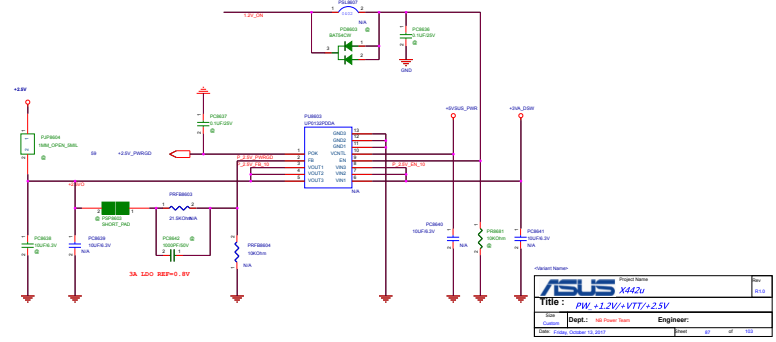


State	Pin7(S3)	Pin8(S6)	VDDQ	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	OFF(HI-Z)
S4/S5	0	0	OFF (Discharge)	OFF (Discharge)	OFF (Discharge)

+1.2V/+VTT [For DDR4]

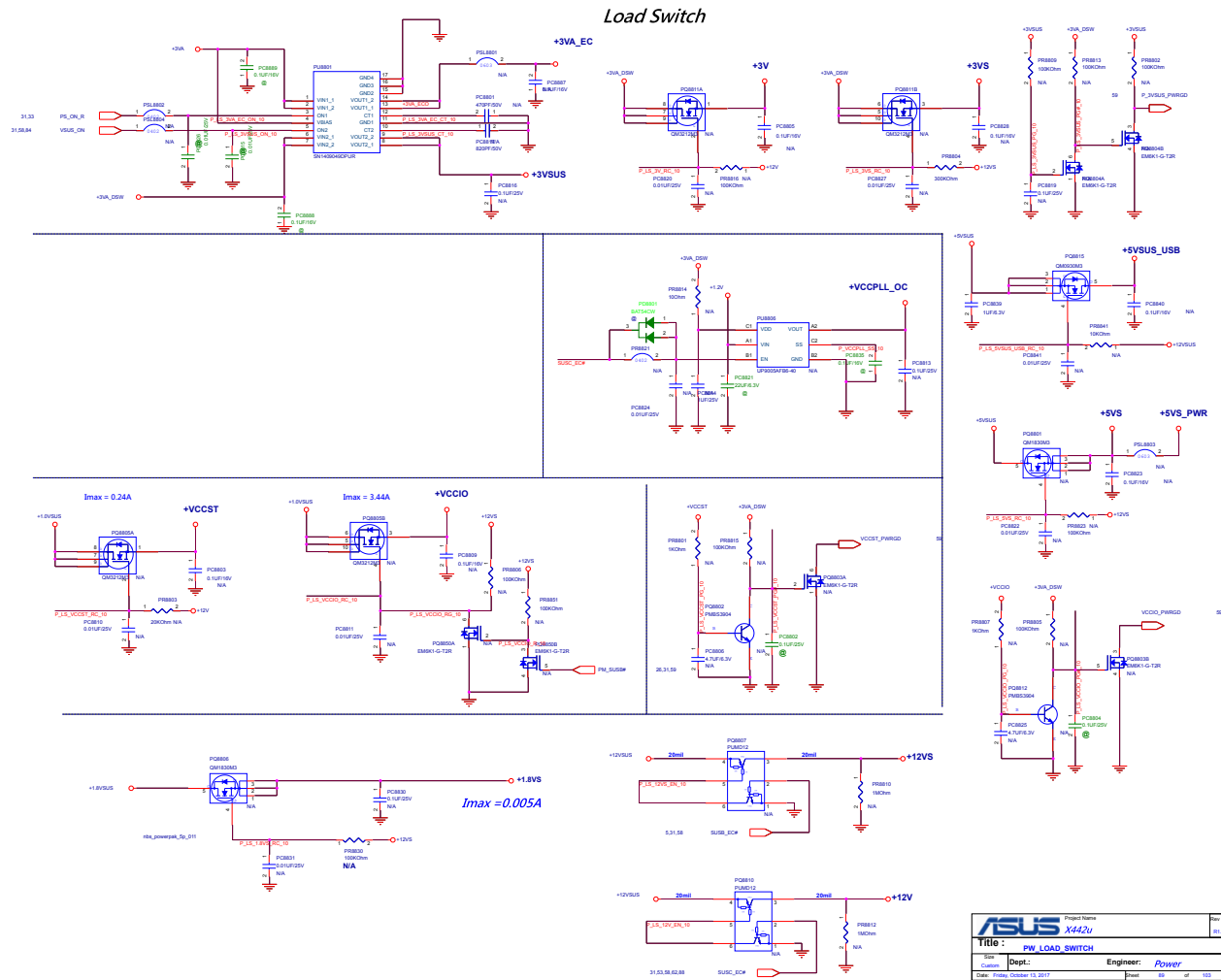


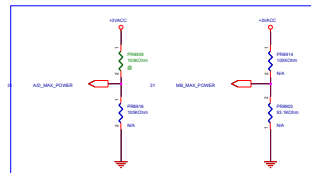
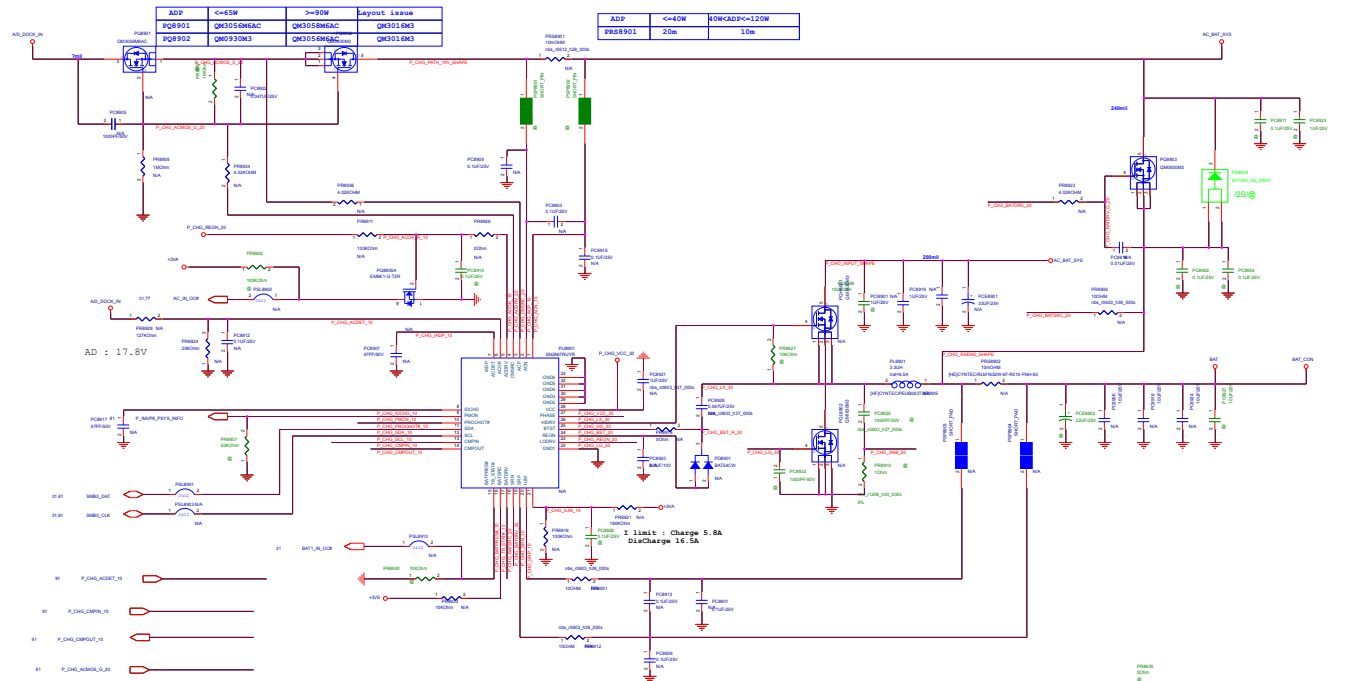
Part Reference	UP156PQKF		UP3002PQKF		RT8248AGQW	
	MLCC	V-CHIP	MLCC	V-CHIP	MLCC	V-CHIP
PR8621	2.2000u	2.2000u	1000u	1000u	@	@
PC8622	1uF	1uF	@	@	0u00u	0u00u
PR8609	@	@	3000u	3000u	@	@
PR8607	8200u	8200u	5600u	5600u	6200u	6200u
PR8604	1700u	4000u	1000u	@	1700u	@
PC8613	820pF	820pF	1000pF	@	820pF	@
PR8623	1500u	1500u	1500u	@	@	@
PR8630	@	@	@	@	1500u	1500u



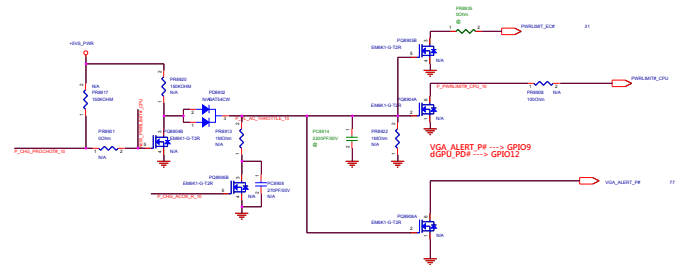
Project Name: 
 Title: 
 Date: 
 Dept: 
 Engineer:





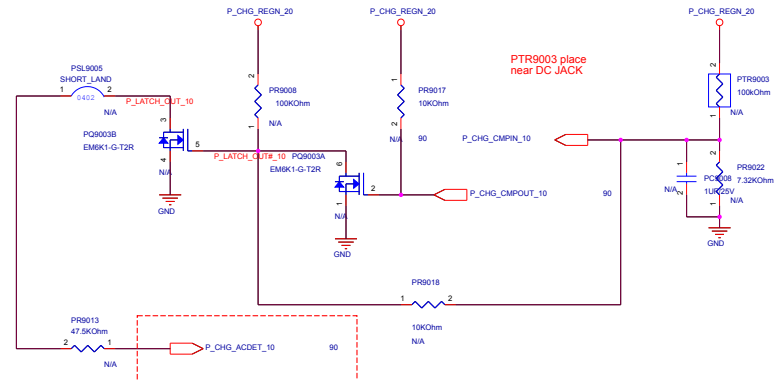
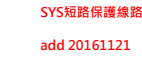


Adaptor select			
		5 Series	6 Series
PRB901		10m	5m
PRB903			
14K	0.4V	30W	120W
31.6K	0.8V	40W	150W
56K	1.2V	45W	180W
93.1K	1.6V	65W	230W
150K	2.0V	75W	300W
270K	2.4V	90W	330W
560K	2.8V	120W	400W

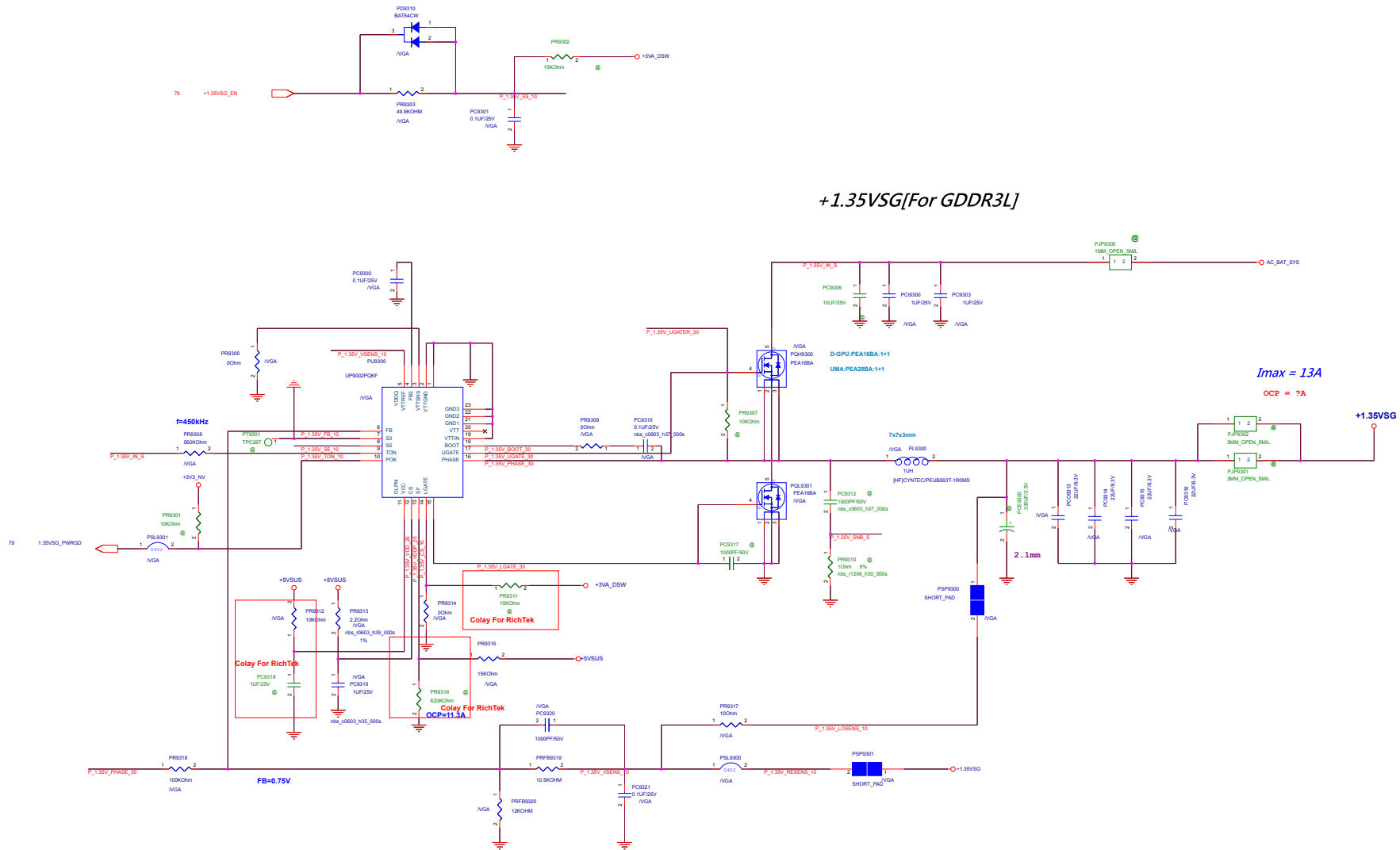


Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9001	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9002	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
R/W	R	R	R	R	R	R	R
Function	Temp. alert threshold setting			Sensed temp. data			bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert







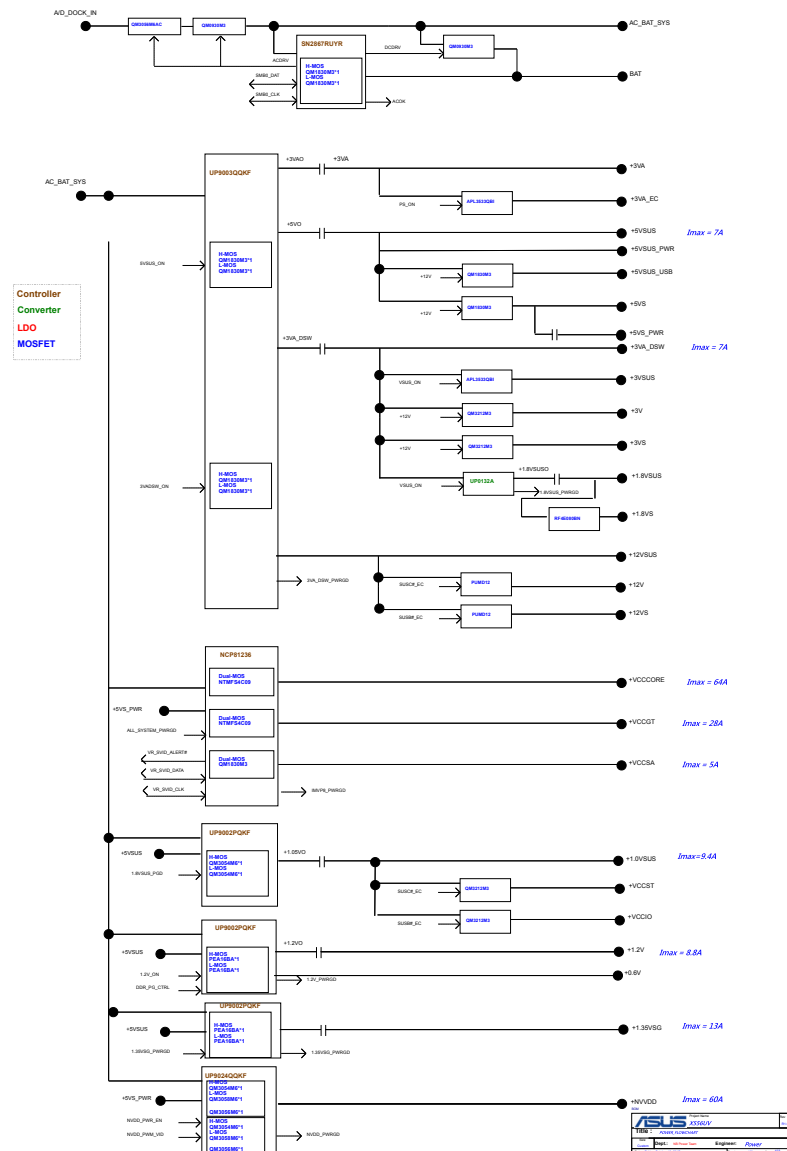
+1.35VSG[For GDDR3L]

$I_{max} = 13A$

$OCP = 7A$

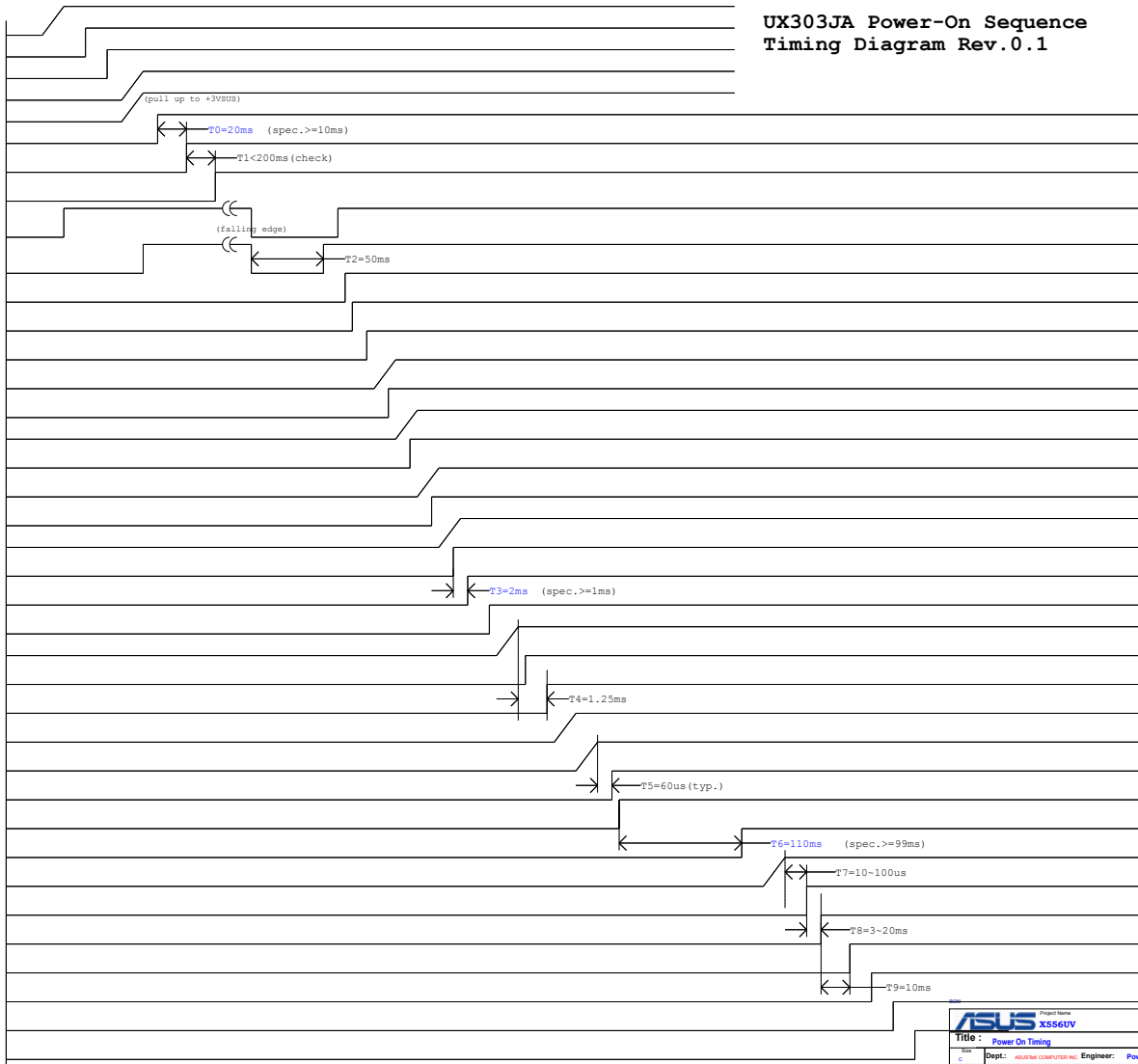
Project Name		Rev
ASUS X442u		R1.0
Title: PW +1.35V/+0.675VS		
Size	Dept.: NB Power Team	Engineer:
Custom		
Date: Friday, October 13, 2017	Sheet 04	of 103





AC-IN Mode

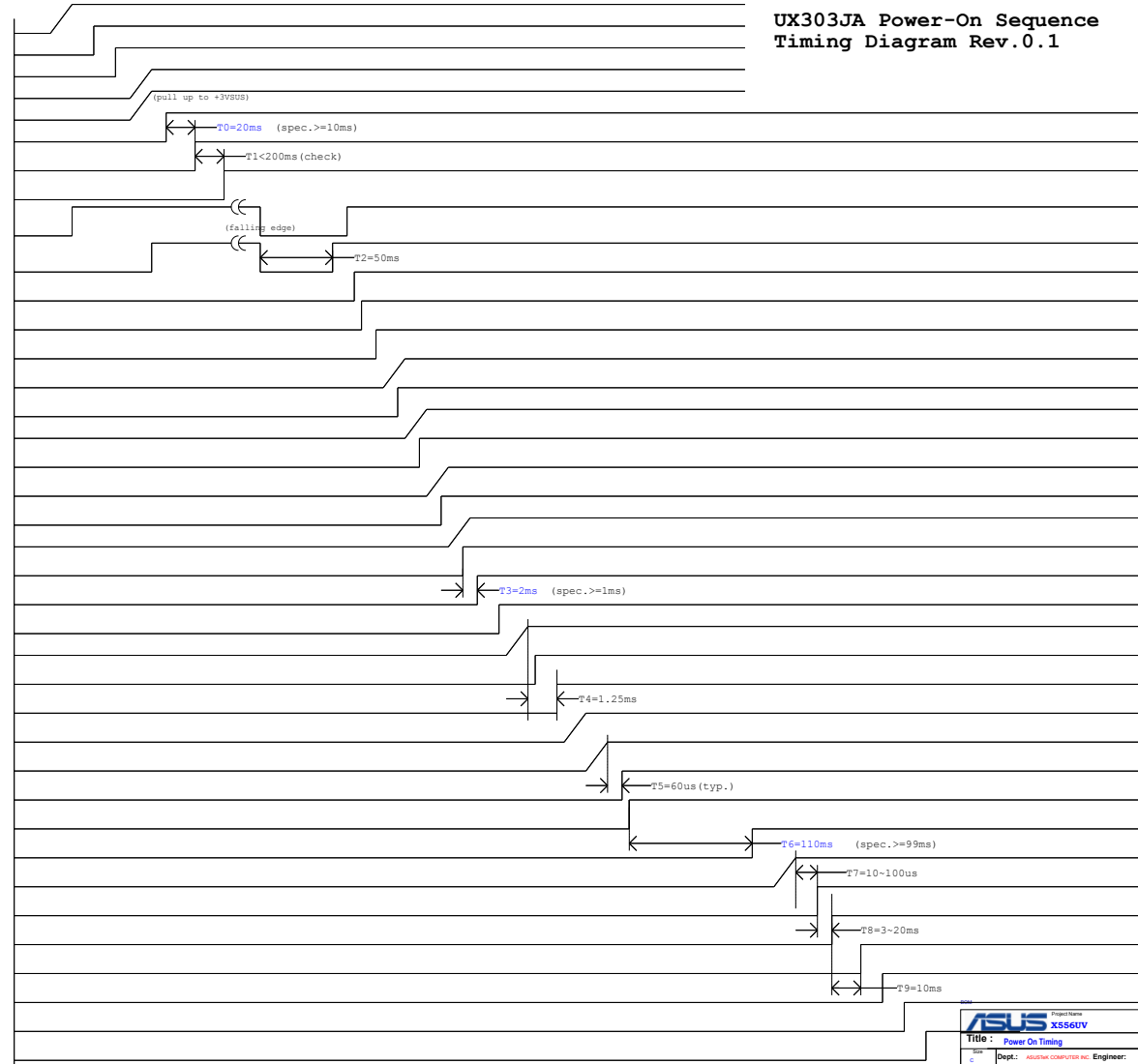
- 1 +3VA/+5VA/+3VA\_EC  
(to EC) 2 EC\_RST#  
(EC to power) 3 VSUS\_ON  
+3VSUS/+5VSUS  
(pull up to +3VSUS)  
(PCH to EC) 4 ME\_SusPwrDrAck  
(power to EC) 5 SUS\_PWRGD  
(EC to PCH) 6 PM\_RSMRST#  
(EC to PCH) 7 AC\_PRESENT  
(to EC) 8 PWR\_SW#  
(EC to PCH) 9 PM\_PWRBTN#  
(PCH to EC) 10 PM\_SLP\_A#  
(PCH to EC) 11 PM\_SUSC#  
12 PM\_SUSB#/SLP\_LAN#  
(PCH to EC) (PCH to power)  
+1.1VM\_LAN  
(EC to power) ME\_SLP\_M\_EC#  
+1.1VM/+3VM  
(EC to power) 13 SUSC\_EC#  
+0.6V/+1.2V/+1.8V/+3V/+5V  
(EC to power) 14 SUSB\_EC#  
+1.05VS/+1.2VS//+1.8VS/+3VS/+5VS  
(power to EC) ME\_VM\_PWRGD  
(EC to PCH) ME\_PWROK  
15 SYSTEM\_PWRGD  
+VTT\_CPU  
(CPU to power) GFX\_VR\_ON  
16 +VTT\_CPU\_PWRGD/ 17 H\_VTT\_PWRGD  
(power to CPU) GFX\_VID  
+VGFX\_CORE  
(power to EC) GFX\_PWRGD  
18 ALL\_SYSTEM\_PWRGD  
(EC to power) CPU\_VRON  
19 +VCCIN  
CLK\_PWRGD  
(inversion of CLK\_EN#)  
(power to EC) 20 CORE\_PWRGD  
(EC to PCH) 21 PM\_PWROK  
(PCH to CPU) H\_DRAM\_PWRGD  
(PCH to CPU) H\_CPUPWRGD  
(PCH to CPU) 22 BUF\_PLT\_RST#



UX303JA Power-On Sequence  
Timing Diagram Rev.0.1

# AC-IN Mode

**1** +3VA/+5VA/+3VA\_EC  
 (to EC) **2** EC\_RST#  
 (EC to power) **3** VSUS\_ON  
 +3VSUS/+5VSUS  
 (PCH to EC) **4** ME\_SusPwrDnAck  
 (power to EC) **5** SUS\_PWRGD  
 (EC to PCH) **6** PM\_RSMRST#  
 (EC to PCH) **7** AC\_PRESENT  
 (to EC) **8** PWR\_SW#  
 (EC to PCH) **9** PM\_PWRBTN#  
 (PCH to EC) **10** PM\_SLP\_A#  
 (PCH to EC) **11** PM\_SUSC#  
**12** PM\_SUSB#/SLP\_LAN#  
 (PCH to EC) (PCH to power)  
 +1.1VM\_LAN  
 (EC to power) ME\_SLP\_M\_EC#  
 +1.1VM/+3VM  
 (EC to power) **13** SUSC\_EC#  
 +0.6V/+1.2V/+1.8V/+3V/+5V  
 (EC to power) **14** SUSB\_EC#  
 +1.05VS/+1.2VS//+1.8VS/+3VS/+5VS  
 (power to EC) ME\_+VM\_PWRGD  
 (EC to PCH) ME\_PWROK  
**15** SYSTEM\_PWRGD  
 +VTT\_CPU  
 (CPU to power) GFX\_VR\_ON  
**16** +VTT\_CPU\_PWRGD/ **17** H\_VTT\_PWRGD  
 (power to CPU) GFX\_VID  
 +VGFX\_CORE  
 (power to EC) GFX\_PWRGD  
**18** ALL\_SYSTEM\_PWRGD  
 (EC to power) CPU\_VRON  
**19** +VCCIN  
 CLK\_PWRGD  
 (inversion of CLK\_EN#)  
 (power to EC) **20** CORE\_PWRGD  
 (EC to PCH) **21** PM\_PWROK  
 (PCH to CPU) H\_DRAM\_PWRGD  
 (PCH to CPU) H\_CPU\_PWRGD  
 (PCH to CPU) **22** BUF\_PLT\_RST#

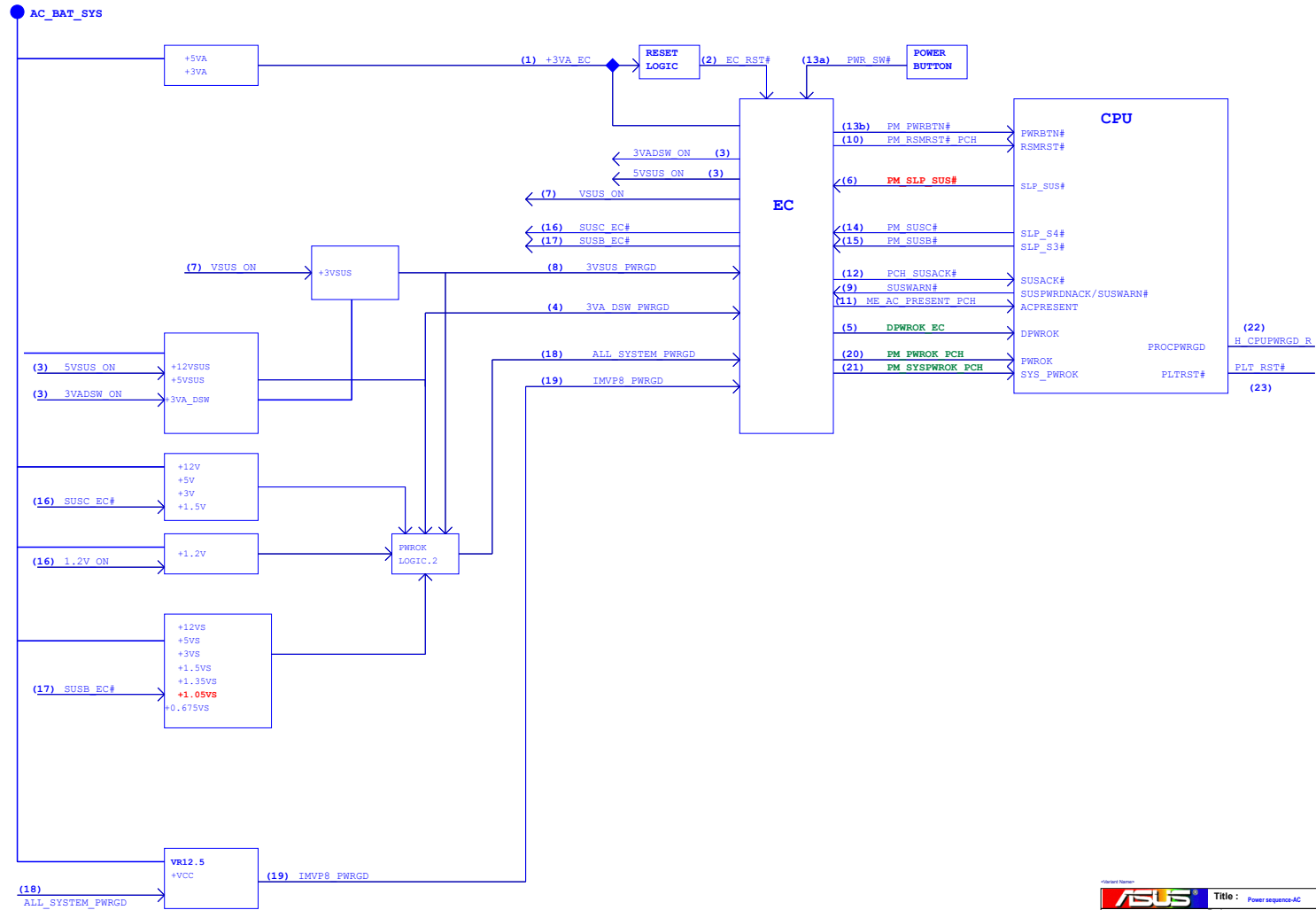


## UX303JA Power-On Sequence Timing Diagram Rev.0.1

ASUS		Project Name	Rev.
X5560V			01.1
Title : Power On Timing			
Size	Dept. : ASUS COMPUTER INC.	Engineer : Power	
Date : 2016. 10. 20	Drawn : 102	Chk : 102	

AC-IN Mode

## X556U Power On Sequence Diagram



Related Diagrams

ASUS		Title : Power sequence-AC	
ASUS/No Computer Inc.		Engineer: nlc	
Rev	Project Name	Rev	Rev
0	X556UV		0.1
Date : 2008.10.20		Page : 101 of 101	